Data Sheet

WE® DSP32 Digital Signal Processor

Description

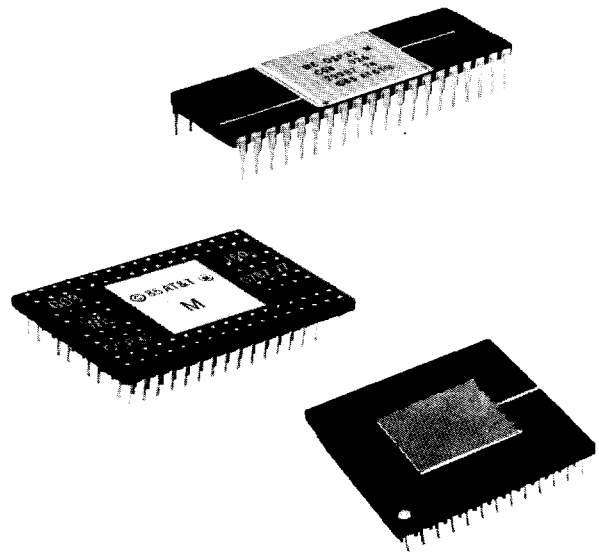


Photo is not actual size.

The *WE* DSP32 Digital Signal Processor integrated circuit is a 32-bit high-speed programmable digital signal processor. The device is available in two versions, at 16 MHz or 25 MHz. Both 16-MHz and 25-MHz parts are available in three packages: a standard 40-pin DIP, a 100-pin rectangular pin-grid-array (PGA) package, and a 13- x 13-pin square PGA package. High throughput is achieved by using two execution units, the control arithmetic unit (CAU) and the data arithmetic unit (DAU). The CAU is a 16-bit fixed-point unit for logic and control, and the DAU is a 32-bit floating-point unit for signal processing algorithms. The CAU includes twenty-one 16-bit general-purpose registers and can execute 6.25 million instructions per second at 25 MHz. The DAU contains a floating-point multiplier and adder, and four 40-bit accumulators. The DAU is configured for multiply/accumulate and can perform 12.5 million floating-point computations per second at 25 MHz. The on-chip memory includes 2048 bytes of ROM and 4096 bytes of RAM. Memory can be addressed as 8-, 16-, or 32-bit words and is organized to access 32-bit data at the same speed as 8-bit data. With the PGA packages, memory can be expanded off-chip with 56 Kbytes of directly accessible data. The device has three I/O ports: a serial port, a parallel port to interface with a microprocessor, and an external memory interface (PGA packages only) for memory-mapped I/O.

Features

- 16-MHz and 25-MHz parts are available
- 2048 bytes ROM, 4096 bytes RAM (on-chip)
- Memory can be addressed as 8, 16, or 32 bits
- Four 40-bit accumulators
- Off-chip memory expansion of up to 56 Kbytes (PGA packages only)
- Four memory accesses per instruction cycle
- 32-bit floating-point arithmetic
- 16-bit integer operations
- Interfaces to a microprocessor without any additional devices
- Serial and parallel I/O ports with DMA options
- Error control logic
- Single 5 V power supply required
- Supported by *WE* DSP32-CC C Language Compiler, *WE* DSP32-SL Support Software Library, *WE* DSP32-AL Application Software Library and *WE* DSP32-DS Digital Signal Processor Development System

User Information

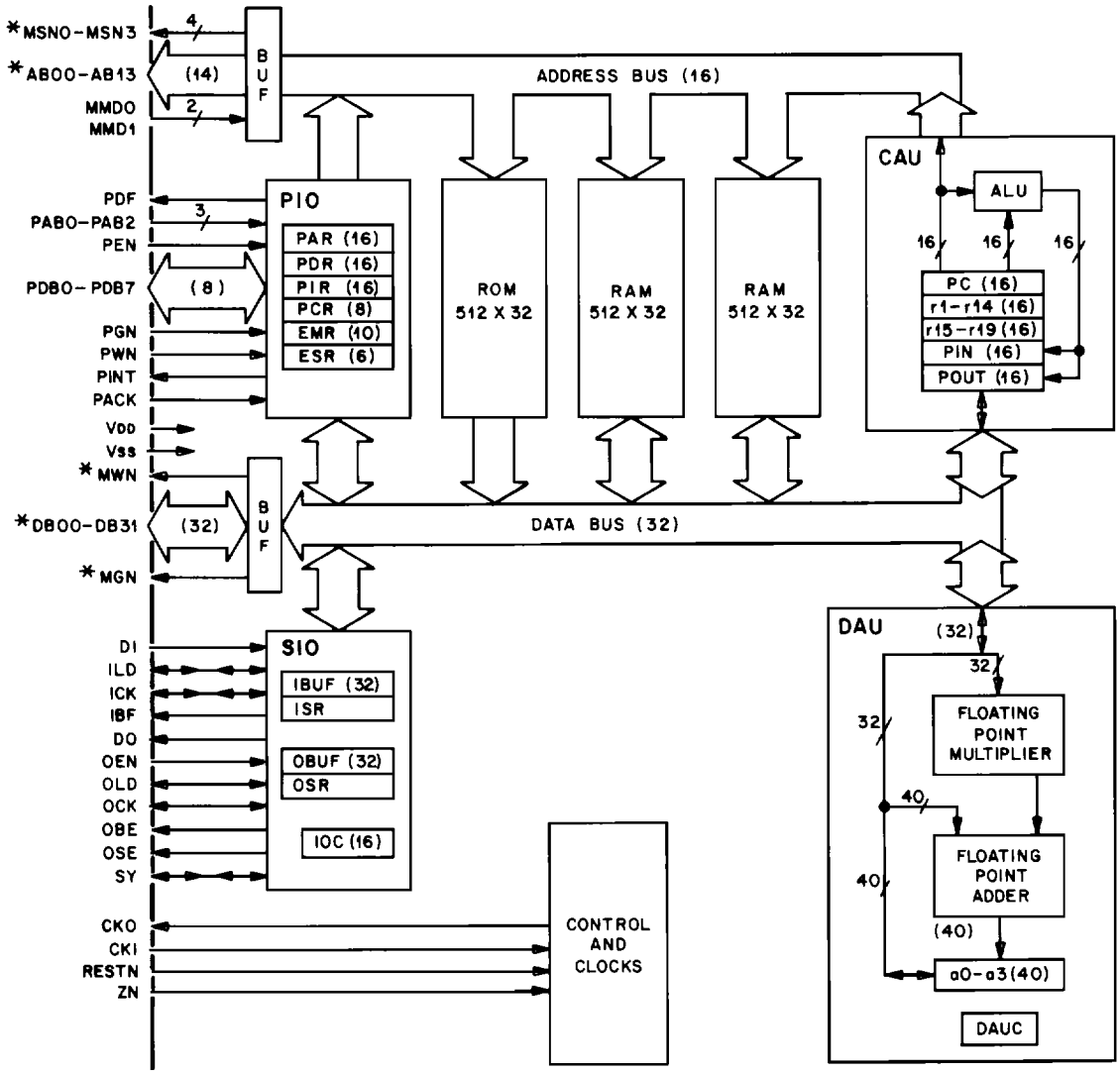
Architectural Summary

The control arithmetic unit (CAU) is used to generate memory addresses and to execute 16-bit integer operations (see Figure 1). The CAU can execute 6.25 million instructions per second and has twenty-one 16-bit registers, a 16-bit program counter (PC), and an arithmetic logic unit (ALU). All CAU registers are static and do not require refreshing. When addressing 32-bit floating-point operands, registers r1—r14 are used as memory pointers (rP), and r15—r19 are used as increment registers (rI). Register r20, also called PIN (parallel input register), is used as the serial input/output (SIO) DMA input pointer. Register r21, also called POUT (parallel output register), is used as the SIO DMA output pointer. All registers can be general-purpose in the execution of the 16-bit integer operations.

The data arithmetic unit (DAU) is configured for multiply/accumulate operations and is the primary execution unit for signal processing algorithms. The DAU contains a floating-point multiplier and adder and four 40-bit accumulators (a0—a3). The DAU can perform 6.25 million instructions per second of the form a = b + c * d. The DAU multiplier inputs are 32-bit floating-point numbers; each number is made up of a 24-bit mantissa and an 8-bit exponent. The adder inputs from memory or an accumulator are 32 or 40 bits. The 40-bit input comes from either an accumulator (a0—a3) or the multiplier (32 bits, plus 8 guard bits). The DAU performs floating-point to-and-from 16-bit integer and floating-point to-and-from μ-law and A-law data type conversions.

The DSP32 device has on-chip memory – 2048 bytes of mask-programmable ROM and 4096 bytes of RAM. Data can be 8-, 16-, or 32-bits wide and memory is uniformly byte-addressable (see the Memory Addressing section). The RAM is dynamic and is refreshed either automatically or under program control. The ROM can be mask-programmed with application program(s) or constant data. Instructions can also be located in on-chip RAM or external memory. With the PGA packages, memory can be expanded off-chip by using standard byte-wide memory devices without any additional interfacing devices. The DSP32 device can directly address 14K instructions (32-bit words) when using off-chip memory.

The DSP32 memory is divided into two banks – a lower bank (0) and an upper bank (1). Memory access can be made without regard to the upper and lower banks. However, to achieve maximum throughput, memory access must alternate between the two memory banks. As one memory bank is accessed, the other memory bank is addressed. This form of pipelining can reduce the effective memory access time by one-half. Only the lower memory bank address space is expandable off-chip. Therefore, the external address and data buses need to operate at only half the rate of the on-chip buses. Pins MMD0 and MMD1 allow the user to select the location of internal ROM and RAM in the memory address space.



Note: See Tables 21—27 for signal name definitions.
* Not available on the 40-pin DIP.

Legend:					
a0—a3	Accumulators 0—3	FPM	Floating-Point Multiplier	PCR	PIO Control Register
ALU	Arithmetic Logic Unit	IBUF	Input Buffer	PDR	PIO Data Register
CAU	Control Arithmetic Unit	IOC	Input/Output Control Register	PIO	Parallel I/O Unit
DAU	Data Arithmetic Unit			PIR	PIO Interrupt Register
DAUC	Data Arithmetic Unit Control Register	ISR	Input Shift Register	r1—r19	Registers 1—19
		OBUF	Output Buffer	PIN	Parallel Input Register
EMR	Error Mask Register	OSR	Output Shift Register	POUT	Parallel Output Register
ESR	Error Source Register	PAR	PIO Address Register	RAM	Read/Write Memory
FPA	Floating-Point Adder	PC	Program Counter	ROM	Read-Only Memory
				SIO	Serial I/O Unit

Figure 1. Block Diagram

The serial I/O (SIO) unit is used for serial-to-parallel conversion of input data and parallel-to-serial conversion of output data. Input to the SIO is loaded into the input shift register (ISR) and then into the input buffer (IBUF). Outputs from the SIO are loaded into the output buffer (OBUF) and then into the output shift register (OSR). This double buffering is done so that back-to-back transfers are possible, which allows the DSP32 program to begin a second transfer before the first has been completed. Data widths can be 8, 16, or 32 bits. The input/output control (IOC) register in the SIO is used to select various I/O conditions, bit lengths, internal or external clock, and internal or external sync (see Table 2).

The parallel I/O (PIO) unit is used for bidirectional communication between the DSP32 device and an external microprocessor. The external PIO data bus is 8-bits wide, and transfers can be made under program or DMA control. The PIO DMA allows a microprocessor to download a program without interrupting the execution of a DSP32 program in progress. The PIO has three 16-bit registers (PAR, PDR, and PIR), a 10-bit register (EMR), an 8-bit register (PCR), and a 6-bit register (ESR). These registers are used to control PIO transfers and to check for errors.

Memory Addressing

A 32-bit memory location can be addressed as one 32-bit floating-point word, two 16-bit integer words, or four 8-bit byte words. A 32-bit memory address is always divisible by four; a 16-bit memory address is divisible by two.

32-Bit Memory Locations				
32-Bit Floating-Point Word				Memory Address
16-Bit Integer		16-Bit Integer		
Byte	Byte	Byte	Byte	
3	2	1	0	0
7	6	5	4	4
11	10	9	8	8
etc.				

Data Type Memory Select				
Data Type	MSN3	MSN2	MSN1	MSN0
Byte 0	1	1	1	0
Byte 1	1	1	0	1
Byte 2	1	0	1	1
Byte 3	0	1	1	1
Low integer	1	1	0	0
High integer	0	0	1	1
Float	0	0	0	0

Each 32-bit word is organized as four bytes, e.g., 3, 2, 1, 0, where byte 3 is the MSByte (most significant byte) and byte 0 is the LSByte (least significant byte). A 16-bit word is 2 bytes, either 1, 0 with byte 1 the MSByte and byte 0 the LSByte, or 3, 2 with byte 3 the MSByte and byte 2 the LSByte. Memory address 0 can refer to an 8-bit word (byte 0), a 16-bit word (1, 0), or a 32-bit word (3, 2, 1, 0).

Memory addresses 00000—57343 (0x0000—0xDFFF)* are in bank 0; memory addresses 57344—65535 (0xE000—0xFFF) are in bank 1. MMD0 and MMD1 are used to select the memory configuration, i.e., the location of the internal RAM and ROM within the address space. Table 1 and Figure 2 show how the memory is configured in the four different memory modes. In all four configurations, the first instruction executed after reset is at address 00000 (0x0000).

Pin-Grid-Array (PGA) Packages

The 14-bit address bus selects a 32-bit word. MSN0—MSN3 (active low) are derived internally according to the data type implied in the instruction and are used to select bytes within that 32-bit word. The two least significant bits of the register pointer (pc, r1—r21) or the direct address determine the values of the memory select lines (MSN0—MSN3). With 56 Kbytes of external memory attached, direct referencing can be made to 65536 bytes, 32768 integers, or 16384 floats. With no external memory, 6144 bytes, 3072 integers, or 1536 floats can be referenced.

* The prefix "0x" indicates hexadecimal notation.

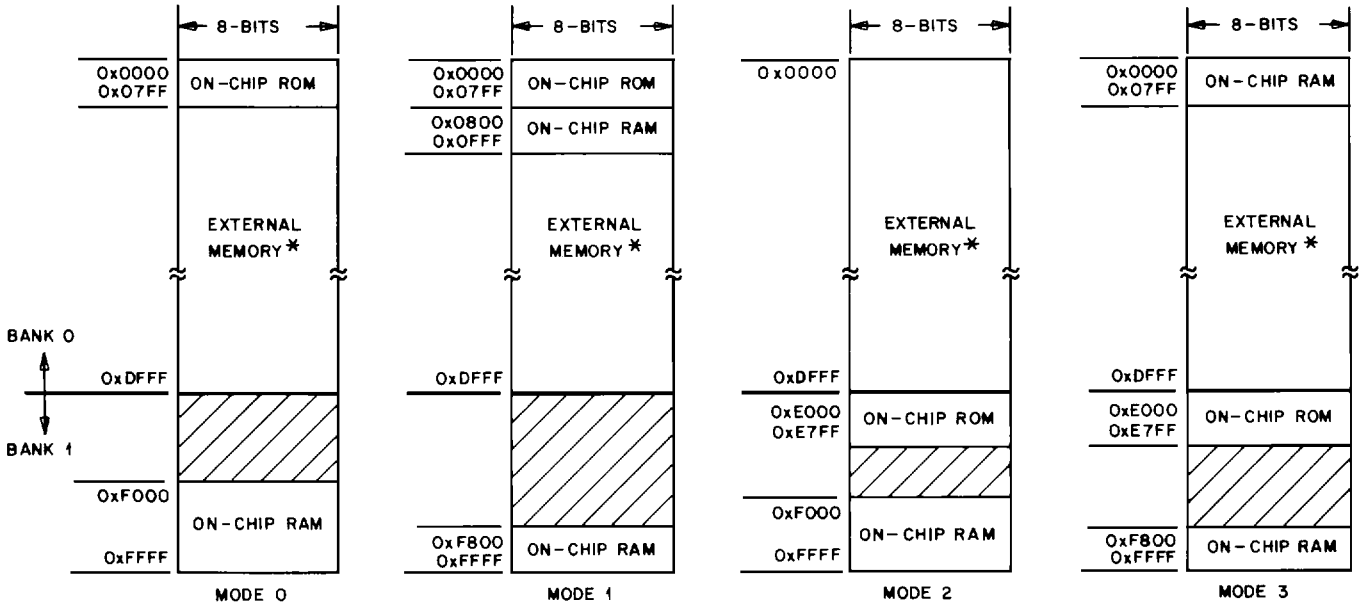
40-Pin Dual In-Line Package (DIP)

On the 40-pin package, the external memory interface (EMI) is not available, limiting total memory to the 512 32-bit words of ROM and 1024 32-bit words of RAM provided on-chip, which can store 4096 bytes, 2048 integers, or 1024 floats.

Table 1. Memory Configuration Selection

Mode	MMD1	MMD0	Addresses	Assignments
0	0	0	0x0000—0x07FF 0x0800—0xDFFF 0xF000—0xFFFF	On-chip ROM External memory* On-chip RAM
1	0	1	0x0000—0x07FF 0x0800—0x0FFF 0x1000—0xDFFF 0xF800—0xFFFF	On-chip ROM On-chip RAM External memory* On-chip RAM
2	1	0	0x0000—0xDFFF 0xE000—0xE7FF 0xF000—0xFFFF	External memory* On-chip ROM On-chip RAM
3	1	1	0x0000—0x07FF 0x0800—0xDFFF 0xE000—0xE7FF 0xF800—0xFFFF	On-chip RAM External memory* On-chip ROM On-chip RAM

* External memory not available on the 40-pin DIP.



* External memory not available on the 40-pin DIP.

Figure 2. Memory Address Configurations

Register Operation

The following tables show the register settings for various operating conditions of the *WE* DSP32 Digital Signal Processor.

IOC and DAUC Registers

Tables 2 and 3 show the operating conditions that result after setting the IOC and DAUC registers.

Table 2. IOC Register

Bit	15—13	12	11,10	9	8	7,6	5	4	3,2	1	0
Field	DMA	SAN	OLEN	AOL	AOC	ILEN	AIL	AIC	SLEN	BC	ASY

Bit	Mnemonic	Function
0	ASY	If cleared (0), SY is external; if set (1), SY is internal. If generated internally, SY = {ICK, OCK}/{256, 512, 1024} = IOC[BC]/(32*IOC[SLEN]).
1	BC	If cleared, ICK is used to derive the on-chip load and SY clocks; if set, OCK is used to derive the on-chip load and SY clocks.
3,2	SLEN	These bits select the frequency ratio of the on-chip load clock to the on-chip SY clock: 00 – xx 01 – ratio = 8 10 – ratio = 16 11 – ratio = 32
4	AIC	If cleared, the clock ICK is external; if set, the clock ICK = CKI/8 and is internal.
5	AIL	If cleared, clock ILD is external; if set, clock ILD = {ICK, OCK}/(32) = IOC[BC]/(32) and is internal.
7,6	ILEN	These bits specify the length of the input serial data: 00 – xx 01 – serial input length = 8 bits 10 – serial input length = 16 bits 11 – serial input length = 32 bits
8	AOC	If cleared, OCK is external; if set, OCK = CKI/8 and is internal.
9	AOL	If cleared, OLD is external; if set, OLD = {ICK,OCK}/(32) = IOC[BC]/(32) and is internal.
11,10	OLEN	These bits specify the length of the serial output data: 00 – xx 01 – serial output length = 8 bits 10 – serial output length = 16 bits 11 – serial output length = 32 bits
12	SAN	If cleared, clear sanity; if set, set sanity.

Table 2. IOC Register (Continued)

Bit	Mnemonic	Function
15—13	DMA[2—0]	These bits control DMA mode: 000 – no DMA 001 – input DMA when IBF is high 010 – output DMA when OBE is high 011 – input DMA when IBF is high, output DMA when OBE is high 100 – input and output DMA when both IBF and OBE are high 101 – input and output DMA when IBF is high 110 – input and output DMA when OBE is high 111 – input and output DMA when either IBF or OBE is high

Table 3. DAUC Register Settings

DAUC*	Result
xx0	μ-Law input conversion
xx1	A-law input conversion
x0x	μ-Law output conversion
x1x	A-law output conversion
0xx	No parity check on X operands
1xx	Parity check on X operands

* x = don't care.

PIO Control

The PIO has a processor address bus (PAB0—PAB2) to select the various PIO registers. Table 4 shows the register selection.

Table 4. Register Selection

PAB2—PAB0	Register Selected
000	PAR(l) – lower byte
001	PAR(h) – upper byte
010	PDR(l) – lower byte
011	PDR(h) – upper byte
100	EMR(l) – lower byte; most significant 5 bits
101	EMR(h) – upper byte; most significant 5 bits
110	ESR – most significant 6 bits
111	PCR

Tables 5 and 6 describe PCR and ESR, two of the PIO registers.

The PIO control register (PCR) is an 8-bit register used by an external microprocessor (μP) to set up various controlled transfer modes between the DSP32 device and the microprocessor.

Table 5. PCR Register

Bit	7	6	5	4	3	2	1	0
Field	REF	PIF	PDF	AUTO	DMA	ENI	Intmode	Reset

Bit	Mnemonic	Function
0	Reset	If cleared, halts DSP32 device; if set, runs DSP32 device. Zero-to-one transition initiates reset sequence.
1	Intmode	If cleared, 8-bit PIR interrupt vector; if set, 16-bit PIR interrupt vector.
2	ENI	If cleared, disables PINT due to PIR interrupt; if set, enables PINT due to PIR interrupt.
3	DMA	If cleared, DMA disabled on PIO; if set, DMA enabled on PIO.
4	AUTO	If cleared, PAR not autoincremented on DMA; if set, PAR autoincremented on DMA.
5	PDF	Set when PDR is written to by DSP32 or μP; cleared when PDR is read by DSP32 or μP (read only).
6	PIF	Set when PIR is written to by DSP32 device; cleared when PIR is read by μP (read only).
7	REF	If cleared, enables RAM autorefresh; if set, disables RAM autorefresh.

The error source register (ESR) has 6 bits that can be read only by the external microprocessor. It is cleared after a read. This register is used to store error conditions (bits 3—7) in the DSP32 device.

Table 6. ESR Register

Bit	7	6	5	4	3	2	1	0
Field	LOSY	LOS	ADER	OVE	PE	WPIR	Not Used	

Bit	Mnemonic	Name/Description
0	—	**Not used.**
1	—	**Not used.**
2	WPIR	**PIR Write.** Set when DSP32 device writes to PIR.
3	PE	**Parity Error.** If set, instruction memory parity error.
4	OVE	**Overflow/Underflow Error.** If set, DAU overflow or underflow.
5	ADER	**Addressing Error.** If set, an attempt was made to access a float variable or an integer variable with an address that was not a multiple of 4 or 2, respectively.
6	LOS	**Loss of Sanity.** If set, sanity bit in the IOC register is set and SY changes state from high to low.
7	LOSY	**Loss of Sync.** If set, loss of 8 kHz external sync.

Instruction Set

The DSP32 device has a powerful instruction set for signal processing algorithms, called data arithmetic (DA) instructions. It also supports instructions for logic and control, called control arithmetic (CA) instructions.

DA instructions, which execute in the DAU, perform 32-bit floating-point multiply/accumulate operations for signal processing algorithms. DA instructions also include special functions for such data-type conversions as floating-point to-and-from integer and floating-point to-and-from μ-law and A-law.

CA instructions, which execute in the CAU, are 16-bit integer microprocessor operations that include arithmetic and logic instructions and such control statements as conditional goto and call. CA instructions also include data move statements so that data can be moved between memory, I/O registers, and any of the CAU registers.

Flags

The DSP32 has internal flags that are affected by the results of certain DA, CA, or I/O instructions. These flags, although not directly visible to the user, can be tested by conditional instructions. Table 7 lists the flags, the names used in instructions (see the test column), and the meaning of each flag.

Note: DAU flags are represented with upper case letters, while CAU flags are represented with lower-case letters.

Table 7. DSP32 Flags

DAU Flags				
Flag	**Test (State = 1)**	**Meaning**	**Test (State = 0)**	**Meaning**
N	alt	Result is negative	age	Result not negative
Z	aeq	Result is zero	ane	Result not zero
V	avs	Result overflowed	avc	No overflow
U	aus	Result underflowed	auc	No underflow
CAU Flags				
n	mi	Result is negative	pl	Result not negative
z	eq	Result is zero	ne	Result not zero
v	vs	Result overflowed	vc	No overflow
c	cs	Carry or borrow out of MSB	cc	No carry or borrow
I/O Flags				
i	ibf	Input buffer full	ibe	Input buffer empty
o	obf	Output buffer full	obe	Output buffer empty
p	pdf	Parallel data register full	pde	PDR empty
P	pif	Parallel interrupt register full	pie	PIR empty
s	sys	SY (I/O sync pulse) set	syc	SY cleared
b	fbs	Serial I/O frame boundary	fbc	Not SIO frame boundary

For example, for testing the U flag (state is 1) there is an instruction:

if(aus) goto *address*

Flags shown at the end of an instruction indicate which flags are affected by the result of that instruction.

A zero (0) shown in place of a flag means that the flag is always 0; a dash (–) in place of a flag means that the flag is unaffected by the instruction.

Instructions

The following is the complete DSP32 instruction set, grouped as DA and CA instructions. Where braces, {}, are shown in an instruction, one of the enclosed items must be chosen. Items enclosed in brackets [ ] are optional.

Note: {} and [ ] are not part of the instruction syntax. Parentheses, ( ), are part of the syntax and must appear where shown in an instruction. Lower-case letters are part of the syntax. Upper-case letters are replaced by immediate data or by a register name (see tables following each instruction group).

Data Arithmetic (DA) Instructions

The DA instructions are divided into two functional groups: multiply/accumulate and special functions.

Table 8. DA Multiply/Accumulate Instructions

Instruction	DAU Flags Affected	Description
[Z=] aN = [–]aM {+,–} Y* X	NZVU	The product of the X and Y fields is added/subtracted to/from the accumulator (aM) and the result is stored in an accumulator (aN). The result can also be output according to the Z field.
aN = [–]aM {+,–} (Z=Y)* X	NZVU	The Y field operand is output according to the Z field. The product of the X and Y fields is added to the accumulator (aM) and the sum is stored in an accumulator (aN).
[Z=] aN = [–]Y {+,–} aM* X	NZVU	The product of the X field and the accumulator (aM) is added/subtracted to/from the Y field. The result is placed in an accumulator (aM) and can also be output according to the Z field.
[Z=] aN = [–]Y* X	NZVU	The product of the X and Y fields is added/subtracted to/from zero. The result is stored in aN and can also be output according to the Z field.
aN = [–](Z=Y)* X	NZVU	The value of the Y field is output according to the Z field. The product of the Y and X fields is stored in an accumulator (aN).
[Z=] aN = [–]Y {+,–}X	NZVU	The sum or difference of the Y and X fields is stored in an accumulator (aN) and the result output according to the Z field. **Note:** X is a multiplier input.
[Z=] aN = [–]Y	NZVU	The value of the Y field is placed in accumulator (aN) and also output according to the Z field.

Table 9. Replacement Table for DA Multiply/Accumulate Instructions

Replace	Value	Meaning
aN, aM, X, Y	a0—a3	One of four DAU accumulators
X,Y,Z	*rP, *rP++, *rP––, *rP++rI	32-bit memory location where rP is a memory pointer (P = 1 – 14) and rI is an increment register (1 = 15 – 19)
X, Y	ibuf	SIO input buffer
Z	obuf	SIO output buffer

Table 10. DA Special Functions

Instruction	DAU Flags Affected	Description
[Z=] aN = ic(Y)	NZ00	Input conversation: μ-law/A-law to float
[Z=] aN = oc(Y)	—	Output conversation: float to μ-law/A-law
[Z=] aN = float(Y)	NZ00	Conversion: integer to float
[Z=] aN = int(Y)	—	Conversion: float to integer
[Z=] aN = round(Y)	NZVU	Conversion: float(40) to float(32)
[Z=] aN = ifalt(Y)	—	If(alt) then [Z=] aN=Y else [Z=] aN

Table 11. Replacement Table for DA Special Function Instructions

Replace	Value	Meaning
aN, Y	a0—a3	One of four DAU accumulators
Y,Z	*rP, *rP++, *rP––, *rP++rI	Memory location where rP is a memory pointer (P = 1 – 14) and r1 is an increment register (1 = 15 – 19)
Y,Z	pdr	PIO data register
Y	ibuf	SIO input buffer
Z	obuf	SIO output buffer

Control Arithmetic (CA) Instructions

The CA instructions are divided into three functional groups: control, arithmetic/logic, and data move.

Table 12. CA Control Group Instructions

Instruction	Flags Affected	Description
if (CA COND) goto {rH, N, rH+N, rH–N}	None	Conditional branch
if (rM–– >= 0) goto {rH, N, rH+N, rH–N}		Conditional branch
if (DA COND) goto {rH, N, rH+N, rH–N}		Conditional branch
if (IO COND) goto {rH, N, rH+N, rH–N}		Conditional branch
call {rH, N, rH+N, rH–N} (rM)		Call subroutine
return (rM)		Return from subroutine
goto {rH, N, rH+N, rH–N}		Unconditional branch
[L]*nop		No operation

Table 13. Replacement Table for CA Control Group Instructions, CA Conditions (CA COND)

Value	CAU Flags*	Meaning
pl	n=0	Result is nonnegative (plus)
mi	n=1	Result is negative (minus)
ne	z=0	Result not equal to zero
eq	z=1	Result equal to zero
vc	v=0	Overflow cleared, no overflow
vs	v=1	Overflow set, overflowed
cc	c=0	Carry cleared, no carry
cs	c=1	Carry set, carry
ge	n^v=0	Greater than or equal to
lt	n^v=1	Less than
gt	z|(n^v)=0	Greater than
le	z|(n^v)=1	Less than or equal to
hi	c|z=0	Greater than (unsigned number)
ls	c|z=1	Less than (unsigned number)

* Symbol interpretation: ^ = XOR; | = OR.

Table 14. Replacement Table for CA Control Group Instructions, DA Conditions (DA COND)

Value	DAU Flags	Meaning
ane	Z=0	Not equal to zero
aeq	Z=1	Equal to zero
age	N=0	Greater than or equal to zero
alt	N=1	Less than zero
avc	V=0	Overflow cleared, no overflow
avs	V=1	Overflow set, overflowed
auc	U=0	Underflow cleared, no underflow
aus	U=1	Underflow set, underflowed
agt	N|Z=0	Greater than zero
ale	N|Z=1	Less than or equal to zero

Table 15. Replacement Table for CA Control Group Instructions, I/O Conditions (IO COND)

Mnemonic	Condition	Meaning
ibe	ibf=0	Input buffer empty
ibf	ibf=1	Input buffer full
obe	obe=1	Output buffer empty
obf	obe=0	Output buffer full
pde	pdf=0	Parallel data register empty
pdf	pdf=1	Parallel data register full
pie	pif=0	Parallel interrupt register empty
pif	pif=1	Parallel interrupt register full
syc	sy=0	Sync signal low
sys	sy=1	Sync signal high
fbc	fb=0	Serial frame boundary clear
fbs	fb=1	Serial frame boundary set

Table 16. CA Arithmetic/Logic Group Instructions

Instruction	CAU Flags Affected	Description
rD = rH+N	nzvc	Three operand add
rD = rD+rS	nzvc	Add
rD = rD–rS	nzvc	Right subtract
rD–{N,rS}	nzvc	Compare
rD = {N, rS}–rD	nzvc	Left subtract
rD = rD&{N, rS}	nz00	AND
rD&{N, rS}	nz00	Bit test
rD = rD|{N, rS}	nz00	OR
rD = rD^{N, rS}	nz00	XOR
rD = rS/2	nz0c	Arithmetic right shift
rD = rS>>1	0z0c	Logical right shift
rD = –rS	nzvc	Negate
rD = rS*2	nzvc	Arithmetic left shift

Table 17. CA Data Move Group Instructions

Instruction	CAU Flags Affected	Description
rD = N	nz00	—
{ioc, dauc} = VALUE	—	—
{MEM,*N, obuf} = {rSh, rSl}	—	MEM, *N, and obuf are 8 bits
{MEM,*N, obuf, pdr, pir} = rS	—	MEM, *N, and obuf are 16 bits
rD = {MEM,*N, ibuf, pdr}	nz00	MEM, *N, and ibuf are 16 bits
{rDh, rDl} = {MEM,*N, ibuf}	nz00	MEM, *N, and ibuf are 8 bits

Table 18. Replacement Table for All CA Instructions

Replace	Value	Meaning
rH	pc, r1—r21	One of 21 general-purpose CAU registers, or the program counter
rM,rS,rD	r1—r21	One of 21 CAU registers
rDh rSh	r1—r21	High-order bits (8—15) are moved; low-order bits (0—7) are cleared for rDh and remain unchanged for rSh
rDl, rSl	r1—r21	Low-order bits (0—7) are moved; high-order bits are cleared for rDl and remain unchanged for rSl
MEM	*rP, *rP++, *rP– –, *rP++rI (P,I = 1—21)	16-bit or 8-bit memory location
L	Positive integer	—
N	16-bit integer	—
VALUE	16-bit integer or 3-bit integer	VALUE is a 16-bit number for the ioc word or a 3-bit number for dauc word

Summary of Instructions

Tables 19 and 20 list DA and CA instructions, along with the encoding format numbers and the flags. The formats for each instruction are found in the next section.

Table 19. DA Instructions

Instructions	Format	DAU Flags Affected			
Multiply/Accumulate:					
[Z =] aN = [–]aM {+,–} Y* X	3	N	Z	V	U
aN = [–]aM {+,–} (Z=Y)* X	2	N	Z	V	U
[Z =] aN = [–]Y {+,–} aM* X	1	N	Z	V	U
[Z =] aN = [–]Y* X	3	N	Z	V	U
aN = [–](Z=Y)* X	2	N	Z	V	U
[Z =] aN = [–]Y {+,–} X	1	N	Z	V	U
[Z =] aN = [–]Y	1	N	Z	V	U
Special Functions:					
[Z=] aN = ic(Y)	4	N	Z	0	0
[Z=] aN = oc(Y)	4	—	—	—	—
[Z=] aN = float(Y)	4	N	Z	0	0
[Z=] aN = int(Y)	4	—	—	—	—
[Z=] aN = round(Y)	4	N	Z	V	U
[Z=] aN = ifalt(Y)	4	—	—	—	—

Table 20. CA Instructions

Instructions	Format	CAU Flags Affected			
Control Group:					
if (CA COND) goto {rH, N, rH+N, rH–N}	0	—	—	—	—
if (rM– –>=0) goto {rH, N, rH+N, rH–N}	3	—	—	—	—
if (DA COND) goto {rH, N, rH+N, rH–N}	0	—	—	—	—
if (IO COND) goto {rH, N, rH+N, rH–N}	1	—	—	—	—
call {rH, N, rH+N, rH–N} (rM)	4	—	—	—	—
return (rM)	0	—	—	—	—
goto {rH, N, rH+N, rH–N}	0	—	—	—	—
[L]*nop	0	—	—	—	—
Arithmetic Logical Group:					
rD = rH+N	5	n	z	v	c
rD = rD+rS	6a	n	z	v	c
rD = rD–{N, rS}	6a,b	n	z	v	c
rD–{N, rS}	6a,b	n	z	v	c
rD = {N, rS}–rD	6a,b	n	z	v	c
rD = rD&{N, rS}	6a,b	n	z	0	0
rD&{N, rS}	6a,b	n	z	0	0
rD = rD|{N, rS}	6a,b	n	z	0	0
rD = rD^{N, rS}	6a,b	n	z	0	0
rD = rS/2	6a	n	z	0	c
rD = rS>>1	6a	0	z	0	c
rD = –rS	6a	n	z	v	c
rD = rS*2	6a	n	z	v	c
Data Move Group:					
rD = N	5	n	z	0	0
{ioc, dauc} = VALUE	5	—	—	—	—
{MEM, *N, obuf} = {rSh, rSl}	7a,b,c	—	—	—	—
{MEM, *N, obuf, pdr, pir} = rS	7a,b,c	—	—	—	—
rD = {MEM, *N, ibuf, pdr}	7a,b,c	n	z	0	0
{rDh, rDl} = {MEM, *N, ibuf}	7a,b,c	n	z	0	0

DA Instruction Formats

There are four DA instruction formats. Refer to the section on DAU encoding for DA instruction formats for an explanation of each field, except where actual bit values (0, 1) are given.

Format 1.

Bit	31	30	29	28	27	26	25	24	23	22	21	20—14	13—7	6—0
Field	P	0	1	M			—	F	S	N		X	Y	Z

Format 2.

Bit	31	30	29	28	27	26	25	24	23	22	21	20—14	13—7	6—0
Field	P	1	0	M			—	F	S	N		X	Y	Z

Format 3.

Bit	31	30	29	28	27	26	25	24	23	22	21	20—14	13—7	6—0
Field	P	1	1	M			—	F	S	N		X	Y	Z

Format 4.

Bit	31	30	29	28	27	26	25	24	23	22	21	20—14	13—7	6—0
Field	P	1	1	1	1	G				N		—	Y	Z

DAU Encoding for DA Instruction Formats

P Field (Bit 31). Specifies the parity bit. This field maintains an odd number of 1s in the encoding format (odd parity). If the remaining 31 bits of the instruction contain an even number of 1s, the P bit is 1; otherwise, the P bit is 0.

Note: This P field (parity) is not to be confused with the p field used for memory pointers (rP).

G Field. Specifies a data type conversion operation.

G	Operation
0000	ic (input conversion)
0001	oc (output conversion)
0010	float
0011	integer
0100	round
0101	ifalt
0110	Reserved
0111	
1000	
1001	
1010	
1011	
1100	
1101	
1110	
1111	

M Field. Specifies the accumulator used or a constant value.

M	Operand
000	a0
001	a1
010	a2
011	a3
100	0.0
101	1.0
110	Reserved
111	

F Field. Specifies sign of operation.

F	Sign
0	+
1	–

N Field. Specifies the accumulator used.

N	Operand
00	a0
01	a1
10	a2
11	a3

S Field. Specifies sign of operation.

S	Sign
0	+
1	–

X, Y, Z Fields. These fields indicate register direct or register indirect modes. The 7-bit fields are divided into two subfields, p and i (ppppiii). Bits 0—2 of the 7-bit field are labeled i; the i subfield specifies an rI register in the CAU. Bits 3—6 are labeled p; the p field specifies an rP register in the CAU.

p Field. Specifies register indirect: *rP, *rP++, *rP––, *rP++rI.

p	Operand
0000	Selects register direct*
0001	r1
0010	r2
0011	r3
0100	r4
0101	r5
0110	r6
0111	r7
1000	r8
1001	r9
1010	r10
1011	r11
1100	r12
1101	r13
1110	r14
1111	Y(p) when Y(p) = X(p) Z(p) when Z(p) = Y(p)

* See i field (p = 0000).

i Field (p = 0000). Specifies a register direct operation: REG. This is a special case of the i field (when p field equals 0).

i	Operand (p = 0000)
000	a0 – X, Y fields only
001	a1 – X, Y fields only
010	a2 – X, Y fields only
011	a3 – X, Y fields only
100	ibuf – X, Y fields only
101	obuf – Z field only
110	pdr – Y, Z fields (special function only)
111	No write, Z field only

i Field (p ≠ 0000). Specifies register indirect: rI, rP++rI.

i	Operand (p ≠ 0000)
000	0
001	r15
010	r16
011	r17
100	r18
101	r19
110	–4(f), –2(l), –1(b)
111	+4(f), +2(i), +1(b)

CA Instruction Formats

There are seven CA instruction formats. Refer to the section on CAU encoding for CA instruction formats for an explanation of each field, except where actual bit values (0, 1) are given.

Formats 0 and 1. Conditional Branch

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15—0
Field	P	0	0	0	0	C					G	H					N

Format 2. Reserved

Bit	31	30	29	28	27	26	25	0
Field	P	0	0	0	1	0	Reserved	

Format 3. Loop Counter

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15—0
Field	P	0	0	0	1	1	M					H					N

Format 4. Call

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15—0
Field	P	0	0	1	0	0	M					H					N

Format 5. Three Operand Add

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15—0
Field	P	0	0	1	0	1	D					H					N

Format 6a. Arithmetic/Logic Group — Register Source

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15—10	9—5	4—0
Field	P	0	0	1	1	0	0	F				D					—	S	—

Format 6b. Arithmetic/Logic Group — Immediate Operand

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15—0
Field	P	0	0	1	1	0	1	F				D					N

Format 7a. Data Move Group — Direct Memory Address

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15—0
Field	P	0	0	1	1	1	0	T	W		0	H					N

Format 7b. Data Move Group — Pointer Increment, Memory Address

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15—10	9—5	4—0
Field	P	0	0	1	1	1	1	T	W		1	H					—	P	I

Format 7c. Data Move Group — I/O

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15—10	9—5	4—0
Field	P	0	0	1	1	1	1	T	W		0	H					—	00000	R

CAU Encoding for CA Instruction Formats

P Field (Bit 31). Specifies the parity bit. This field maintains an odd number of 1s in the encoding format (odd parity). If the remaining 31 bits of the instruction have an even number of 1s, the P bit is 1; otherwise, the P bit is 0.

Note: This P field (parity) is not to be confused with the p field used for memory pointers (rP).

C Field. Specifies a CA, DA, or I/O condition.

C	Condition	C	Condition	C	Condition
00xxx	**CA**	**01xxx**	**DA**	**10xxx**	**I/O**
00000	No condition	01000	U	10000	ibf
00001	n	01001	N	10001	obe
00010	z	01010	Z	10010	pdf
00011	v	01011	V	10011	pif
00100	c	01100	N|Z	10100	sy
00101	n^v	01101	Reserved	10101	fb
00110	z|(n^v)	01110	Reserved	10110	Reserved
00111	c|z	01111	Reserved	10111	Reserved

T Field. Specifies the direction of a transfer: to or from a register.

T	Operation
0	Data is moved to a register from memory
1	Data is moved to memory from a register

W Field. Specifies the high or low byte or integer data.

W	Description
00	High byte
01	Low byte
1x	Integer

G Field. Specifies whether to branch if the condition specified in the C Field is true or false.

G	Operation
0	Branch if condition = 0 (false)
1	Branch if condition = 1 (true)

F Field. Specifies the arithmetic/logic group function encoding.

F	Operation
0000	rD=rD+rS
0001	rD=rS*2
0010	rD={N,rS}–rD
0011	Reserved
0100	rD=rD–{N,rS}
0101	rD=–rS
0110	Reserved
0111	rD–{N,rS}
1000	rD=rD^{N,rS}
1001	Reserved
1010	rD=D | {N,rS}
1011	Reserved
1100	rD=rS>>1
1101	rD=rS/2
1110	rD=rD&{N,rS}
1111	rD&{N,rS}

S, D, M, or H Fields. Used for register encoding.

S,D,M, or H	Operand
00000	0
00001	r1
00010	r2
00011	r3
00100	r4
00101	r5
00110	r6
00111	r7
01000	r8
01001	r9
01010	r10
01011	r11
01100	r12
01101	r13
01110	r14
01111	Program counter (pc)
10000	0
10001	r15
10010	r16
10011	r17
10100	r18
10101	r19
10110	–4(f),–2(i),–1(b)
10111	+4(f),+2(i),+1(b)
11000	r20 (pin)
11001	r21 (pout)
11010	dauc
11011	ioc
11100	
11101	Reserved
11110	
11111	

P Field. Specifies a register indirect data move: *rP, *rP++, *rP––, *rP++rI.

P	Operand
00000	Selects Format 7C
00001	r1
00010	r2
00011	r3
00100	r4
00101	r5
00110	r6
00111	r7
01000	r8
01001	r9
01010	r10
01011	r11
01100	r12
01101	r13
01110	r14
01111	Reserved
10000	Reserved
10001	r15
10010	r16
10011	r17
10100	r18
10101	r19
10110	Reserved
10111	Reserved
11000	r20 (pin)
11001	r21 (pout)
11010	Reserved
11011	
11100	
11101	
11110	
11111	

I Field. Specifies a register indirect operation.

I	Operand
00000	Reserved
00001	r1
00010	r2
00011	r3
00100	r4
00101	r5
00110	r6
00111	r7
01000	r8
01001	r9
01010	r10
01011	r11
01100	r12
01101	r13
01110	r14
01111	Reserved
10000	0
10001	r15
10010	r16
10011	r17
10100	r18
10101	r19
10110	–2(i), –1(b)
10111	+2(i),+1(b)
11000	r20 (pin)
11001	r21 (pout)
11010	Reserved
11011	
11100	
11101	
11110	
11111	

N Field. Specifies a 16-bit integer included as immediate data or as an address.

R Field (P = 00000). Specifies a register direct operation. This field is valid when the P Field is 0.

R	Operand (P=00000)
00000 00001 00010 00011	Reserved
00100	ibuf
00101	obuf
00110	pdr
00111 01000 01001 01010 01011 01100 01101 01110 01111 10000 10001 10010 10011 10100 10101	Reserved
10110	pir
10111 11000 11001 11010 11011 11100 11101 11110 11111	Reserved

Pin Descriptions

In Tables 21—27, I = input, O = output, and P = power. All DSP32 output pins may be 3-stated. A microprocessor (μP) is used as an example of an external device connected to DSP32 device through the PIO interface.

40-Pin DIP

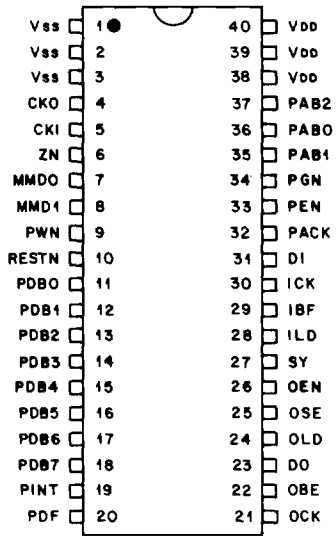


Figure 3. 40-Pin DIP Pin Diagram

Table 21. Pin Descriptions by Numerical Order — 40-Pin DIP

Pin	Symbol	Type	Name/Description
1 2 3	Vss	P	**Ground.**
4	CKO	O	**Clock Out.** Buffered clock at the same frequency as CKI. Synchronizes external devices to the DSP32.
5	CKI	I	**Clock In.** Input clock.
6	ZN	I	**3-State (Active Low).** When active, all DSP32 output pins are 3-stated (high impedance); when not connected, ZN is inactive.
7 8	MMD0 MMD1	I	**Memory Mode — Bits 0 and 1.** Decoded to select the address of on-chip memory (see the Memory Addressing section).
9	PWN	I	**Processor Write Enable (Active Low).** When active, enables on-chip registers to be written to by a μP.
10	RESTN	I	**Reset (Active Low).** Controls the DSP32 run/halt state. A high-to-low transition causes entry into the halt state; a low-to-high transition causes the reset sequence. The reset sequence stores the PC in r14; clears PC, IOC, ESR; and sets EMR to mask all errors. The PCR register bits, except PCR0, are cleared; PCR0 is set. CAU and DAU condition flags and the DAUC register are not affected by reset.

Table 21. Pin Descriptions by Numerical Order — 40-Pin DIP (Continued)

Pin	Symbol	Type	Name/Description
11	PDB0	I/O	**Parallel Data Bus — Bit 0.** Bidirectional 8-bit data bus for μP interface. This bus transfers data into and out of the PIO registers for use by a μP.
12	PDB1		**Parallel Data Bus — Bit 1.**
13	PDB2		**Parallel Data Bus — Bit 2.**
14	PDB3		**Parallel Data Bus — Bit 3.**
15	PDB4		**Parallel Data Bus — Bit 4.**
16	PDB5		**Parallel Data Bus — Bit 5.**
17	PDB6		**Parallel Data Bus — Bit 6.**
18	PDB7		**Parallel Data Bus — Bit 7.**
19	PINT	O	**Processor Interrupt.** Interrupt to μP. PINT is set when a nonmasked error occurs or when the DSP32 writes to PIR and bit 2 of PCR is high; PINT is cleared by reading ESR or PIR.
20	PDF	O	**Parallel Data Full.** Set when PDR is written to by the DSP32 or a μP; cleared when PDR is read by the DSP32 or a μP.
21	OCK	I/O	**Output Clock.** Clock for serial PCM output data. In internal mode OCK is an output; in external mode OCK is an input, depending on the I/O format.
22	OBE	O	**Output Buffer Empty.** Indicates state of serial PCM output buffer (OBUF). OBE is cleared when OBUF is written by the DSP32.
23	DO	O	**Data Output.** Serial PCM data output from OBUF. 3-stated when OEN is high.
24	OLD	I/O	**Output Load.** Clock for loading the parallel-to-serial converter from OBUF. In internal mode OLD is an output; in external mode OLD is an input, depending on the I/O format.
25	OSE	O	**Output Shift Register Empty.** Indicates end of serial transmission. Complement of OLD and delayed by the number of bits in the transmission, as set by the IOC register.
26	OEN	I	**Output Enable (Active Low).** Enables DO as an output. When high, DO is 3-stated.
27	SY	I/O	**Synchronization.** In internal mode (output), DSP32 provides frame sync; in external mode (input), frame sync is provided to the DSP32.
28	ILD	I/O	**Input Load.** Clock for loading input buffer from serial-to-parallel converter. In internal mode ILD is an output; in external mode ILD is an input, depending on the I/O format.
29	IBF	O	**Input Buffer Full.** Indicates state of input buffer (IBUF). IBF is cleared when IBUF is loaded onto the parallel data bus by the DSP32.

Table 21. Pin Descriptions by Numerical Order — 40-Pin DIP (Continued)

Pin	Symbol	Type	Name/Description
30	ICK	I/O	**Input Clock.** Clock for serial PCM input data. In internal mode ICK is an output; in external mode ICK is an input, depending on the I/O format.
31	DI	I	**Data Input.** Serial PCM data into IBUF.
32	PACK	I	**Processor Acknowledge.** Flag from μP acknowledging an interrupt. PACK allows the μP to read PIR register and to reset PINT.
33	PEN	I	**Processor Interface Enable (Active Low).** When active, PEN allows a read from or a write to the processor PIO data bus (PDB).
34	PGN	I	**Processor Read Enable (Active Low).** When active, enables PDB for output and allows the μP to read data from the selected PIO register.
35 36 37	PAB1 PAB0 PAB2	I	**Processor Address Bus — Bits 0—2.** Decoded to select lower or upper byte of PAR, PDR, or EMR. Also selects ESR/PCR.
38 39 40	V_{DD}	P	**5 V Supply.**

100-Pin Rectangular PGA Package

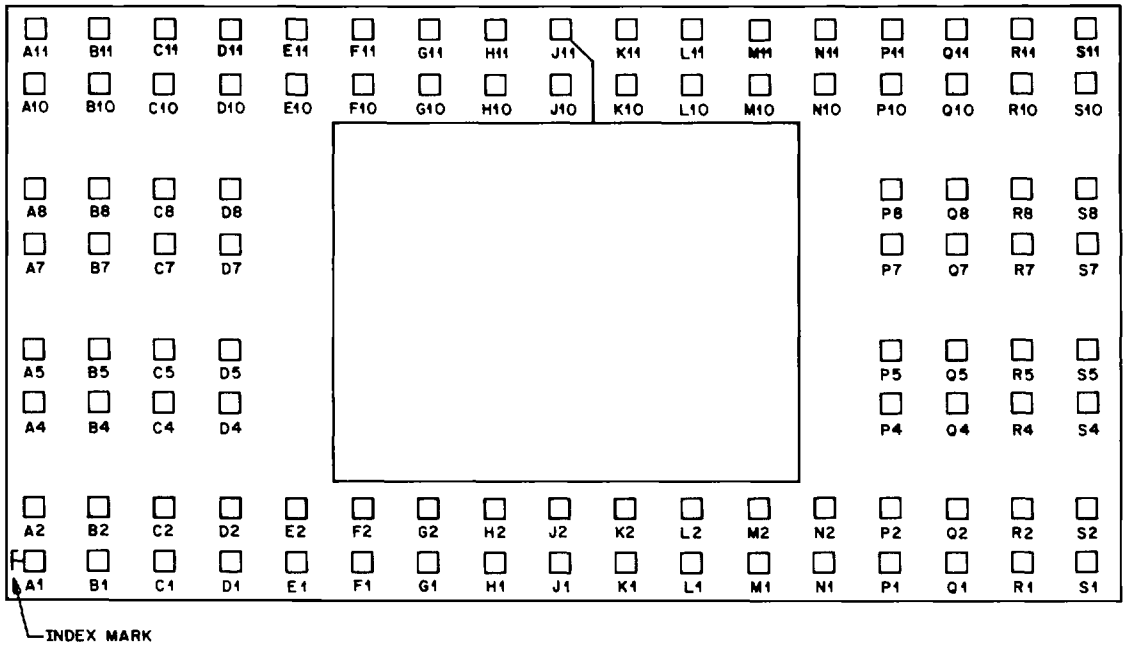


Figure 4. 100-Pin Rectangular PGA Diagram — Top View

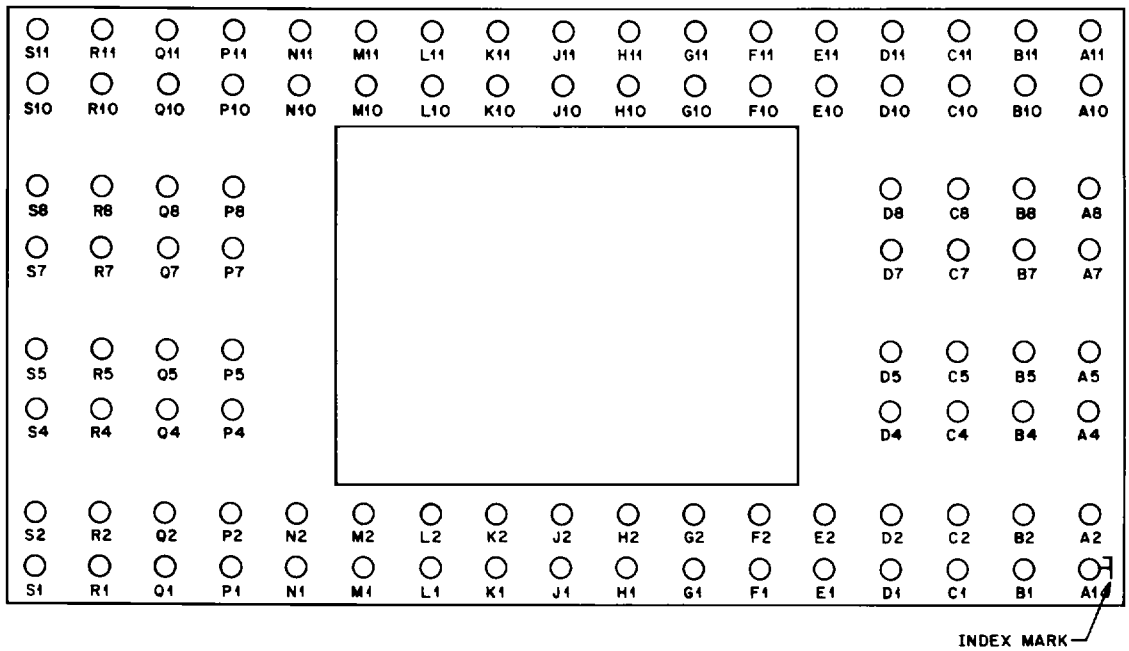


Figure 5. 100-Pin Rectangular PGA Diagram — Bottom View

Table 22. Pin Descriptions by Alphanumerical Order — 100-Pin PGA Package

Pin	Symbol	Type	Name/Description
A1	DB00	I/O	**External Memory Data Bus — Bit 00.**
A2	DB01	I/O	**External Memory Data Bus — Bit 01.**
A4	Vss	P	**Ground.**
A5	MSN1	O	**Memory Select — Bit 1 (Active Low).** Selects byte 1 of memory addressed by the external memory address bus.
A7	MSN0	O	**Memory Select — Bit 0 (Active Low).** Selects byte 0 of memory addressed by the external memory address bus.
A8	Vss	P	**Ground.**
A10	AB07	O	**External Memory Address Bus — Bit 07.**
A11	AB06	O	**External Memory Address Bus — Bit 06.**
B1	DB02	I/O	**External Memory Data Bus — Bit 02.**
B2	DB03	I/O	**External Memory Data Bus — Bit 03.**
B4	MSN3	O	**Memory Select — Bit 3 (Active Low).** Selects byte 3 of memory addressed by the external memory address bus.
B5	MSN2	O	**Memory Select — Bit 2 (Active Low).** Selects byte 2 of memory addressed by the external memory address bus.
B7	AB13	O	**External Memory Address Bus — Bit 13.**
B8	AB12	O	**External Memory Address Bus — Bit 12.**
B10	AB05	O	**External Memory Address Bus — Bit 05.**
B11	AB04	O	**External Memory Address Bus — Bit 04.**

Table 22. Pin Descriptions by Alphanumerical Order — 100-Pin PGA Package (Continued)

Pin	Symbol	Type	Name/Description
C1	DB04	I/O	**External Memory Data Bus — Bit 04.**
C2	DB05	I/O	**External Memory Data Bus — Bit 05.**
C4	—	—	**Not Used.** This pin must be left open.
C5	—	—	**Not Used.** This pin must be left open.
C7	AB11	O	**External Memory Address Bus — Bit 11.**
C8	AB10	O	**External Memory Address Bus — Bit 10.**
C10	AB03	O	**External Memory Address Bus — Bit 03.**
C11	AB02	O	**External Memory Address Bus — Bit 02.**
D1	DB06	I/O	**External Memory Data Bus — Bit 06.**
D2	DB07	I/O	**External Memory Data Bus — Bit 07.**
D4	MGN	O	**Memory Output Enable (Active Low).** Enables memory output on external memory data bus.
D5	MWN	O	**Memory Write (Active Low).** Controls data writes to memory.
D7	AB09	O	**External Memory Address Bus — Bit 09.**
D8	AB08	O	**External Memory Address Bus — Bit 08.**
D10	AB01	O	**External Memory Address Bus — Bit 01.**
D11	AB00	O	**External Memory Address Bus — Bit 00.**
E1	V_{DD}	P	**5 V Supply.** For external memory interface. If external memory is not used, this pin must be connected to V_{SS}.
E2	DB08	I/O	**External Memory Data Bus — Bit 08.**
E10	CKI	I	**Clock In.** Input clock.
E11	V_{DD}	P	**5 V Supply.**
F1	DB09	I/O	**External Memory Data Bus — Bit 09.**
F2	DB10	I/O	**External Memory Data Bus — Bit 10.**
F10	MMD1	I	**Memory Mode — Bit 1.** Decoded with MMD0 to select the address of on-chip memory (see the Memory Addressing section).
F11	MMD0	I	**Memory Mode — Bit 0.** Decoded with MMD1 to select the address of on-chip memory.
G1	DB11	I/O	**External Memory Data Bus — Bit 11.**
G2	DB12	I/O	**External Memory Data Bus — Bit 12.**

Table 22. Pin Descriptions by Alphanumerical Order — 100-Pin PGA Package (Continued)

Pin	Symbol	Type	Name/Description
G10	RESTN	I	**Reset (Active Low).** Controls the DSP32 run/halt state; a high-to-low transition causes entry into the halt state; a low-to-high transition causes the reset sequence. The reset sequence stores PC in r14; clears PC, IOC, ESR; and sets EMR to mask all errors. The PCR register bits, except PCR0, are cleared; PCR0 is set. CAU and DAU condition flags and the DAUC registers are not affected by reset.
G11	ZN	I	**3-State (Active Low).** When active, all DSP32 output pins are 3-stated; when not connected, ZN is inactive.
H1	DB13	I/O	**External Memory Data Bus — Bit 13.**
H2	DB14	I/O	**External Memory Data Bus — Bit 14.**
H10	—	—	**Not Used.** This pin must be left open.
H11	CKO	O	**Clock Out.** Buffered clock at the same frequency as CKI. Synchronizes external devices to the DSP32.
J1	DB15	I/O	**External Memory Data Bus — Bit 15.**
J2	DB16	I/O	**External Memory Data Bus — Bit 16.**
J10	—	—	**Not Used.** This pin must be left open.
J11	Vss	P	**Ground.**
K1	DB17	I/O	**External Memory Data Bus — Bit 17.**
K2	DB18	I/O	**External Memory Data Bus — Bit 18.**
K10	—	—	**Not Used.** This pin must be left open.
K11	PAB2	I	**Processor Address Bus — Bit 2.** Bit 2 of 3-bit address from μP decoded along with PAB0 (pin L11) and PAB1 (pin L10) to select the lower and upper byte of PAR, PDR, or EMR. Also selects ESR/PCR.
L1	DB19	I/O	**External Memory Data Bus — Bit 19.**
L2	DB20	I/O	**External Memory Data Bus — Bit 20.**
L10	PAB1	I	**Processor Address Bus — Bit 1.** Bit 1 of 3-bit address from μP decoded along with PAB0 (pin L11) and PAB2 (pin K11) to select the lower or upper byte of PAR, PDR, or EMR. Also selects ESR/PCR.
L11	PAB0	I	**Processor Address Bus — Bit 0.** Bit 0 of 3-bit address from μP decoded along with PAB1 (pin L10) and PAB2 (pin K11) to select the lower or upper byte of PAR, PDR, or EMR. Also selects ESR/PCR.
M1	DB21	I/O	**External Memory Data Bus — Bit 21.**
M2	DB22	I/O	**External Memory Data Bus — Bit 22.**

Table 22. Pin Descriptions by Alphanumerical Order — 100-Pin PGA Package (Continued)

Pin	Symbol	Type	Name/Description
M10	PWN	I	**Processor Write Enable (Active Low).** When active, enables on-chip registers to be written by a μP.
M11	PGN	I	**Processor Read Enable (Active Low).** When active, enables PDB for output and allows the μP to read data from the selected PIO register.
N1	V_{DD}	P	**5 V Supply.** For external memory interface. If external memory is not used, this pin must be connected to V_{SS}.
N2	DB23	I/O	**External Memory Data Bus — Bit 23.**
N10	PEN	I	**Processor Interface Enable (Active Low).** When active, PEN allows a read from or a write to the PIO data bus (PDB).
N11	V_{DD}	P	**5 V Supply.**
P1	DB24	I/O	**External Memory Data Bus — Bit 24.**
P2	DB25	I/O	**External Memory Data Bus — Bit 25.**
P4	OEN	I	**Output Enable (Active Low).** Enables DO for output. When high, DO is 3-stated.
P5	OBE	O	**Output Buffer Empty.** Indicates the state of serial PCM output buffer (OBUF). OBE is cleared when OBUF is written to by the DSP32.
P7	DI	I	**Data Input.** Serial PCM data input to IBUF.
P8	PDF	O	**Parallel Data Full.** Set when PDR is written to by the DSP32 or a μP; cleared when PDR is read by the DSP32 or a μP.
P10	PACK	I	**Processor Acknowledge.** Flag from μP acknowledging interrupt. PACK allows the μP to read PIR register and to reset PINT.
P11	PDB0	I/O	**Parallel Data Bus — Bit 0.**
Q1	DB26	I/O	**External Memory Data Bus — Bit 26.**
Q2	DB27	I/O	**External Memory Data Bus — Bit 27.**
Q4	DO	O	**Data Output.** Serial PCM data output from OBUF. 3-stated when OEN is high.
Q5	IBF	O	**Input Buffer Full.** Indicates state of input buffer (IBUF). IBF is cleared when IBUF is loaded onto the data bus by DSP32.
Q7	ILD	I/O	**Input Load.** Clock for loading input buffer from serial-to-parallel converter. In internal mode ILD is an output; in external mode ILD is an input, depending on the I/O format.

Table 22. Pin Descriptions by Alphanumerical Order — 100-Pin PGA Package (Continued)

Pin	Symbol	Type	Name/Description
Q8	PINT	O	**Processor Interrupt.** Interrupt to μP. PINT is set when a nonmasked error occurs, or when the DSP32 writes to PIR and bit 2 of PCR is set; PINT is cleared by reading ESR or PIR.
Q10	PDB2	I/O	**Parallel Data Bus — Bit 2.**
Q11	PDB1	I/O	**Parallel Data Bus — Bit 1.**
R1	DB28	I/O	**External Memory Data Bus — Bit 28.**
R2	DB29	I/O	**External Memory Data Bus — Bit 29.**
R4	OSE	O	**Output Shift Register Empty.** Indicates end of serial transmission. Complement of OLD. Delayed by the number of bits in the transmission as set by the IOC register.
R5	SY	I/O	**Synchronization.** In internal mode (output), DSP32 provides frame sync; in external mode (input), frame sync is provided to the DSP32.
R7	ICK	I/O	**Input Clock.** Clock for serial PCM input data. In internal mode ICK is an output; in external mode ICK is an input, depending on the I/O format.
R8	PDB7	I/O	**Parallel Data Bus — Bit 7.**
R10	PDB4	I/O	**Parallel Data Bus — Bit 4.**
R11	PDB3	I/O	**Parallel Data Bus — Bit 3.**
S1	DB30	I/O	**External Memory Data Bus — Bit 30.**
S2	DB31	I/O	**External Memory Data Bus — Bit 31.**
S4	Vss	P	**Ground.**
S5	OLD	I/O	**Output Load.** Clock for loading parallel-to-serial converter from OBUF. In internal mode OLD is an output; in external mode OLD is an input, depending on the I/O format.
S7	OCK	I/O	**Output Clock.** Clock for serial PCM output data. In internal mode OCK is an output; in external mode OCK is an input, depending on the I/O format.
S8	Vss	P	**Ground.**
S10	PDB6	I/O	**Parallel Data Bus — Bit 6.**
S11	PDB5	I/O	**Parallel Data Bus — Bit 5.**

13- x 13-Pin Square PGA Package

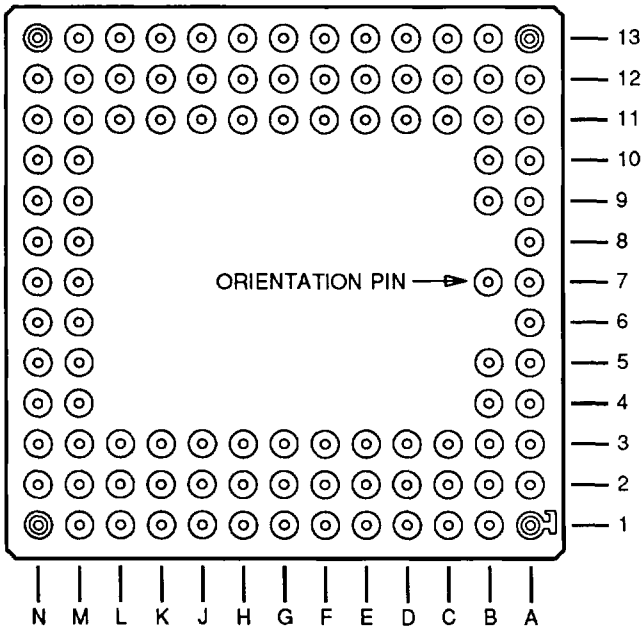


Figure 6. 13- x 13-Pin PGA Diagram — Bottom View

Table 23. Pin Descriptions by Alphanumerical Order — 13- x 13-Pin PGA Package

Pin	Symbol	Type	Name/Description
A1 A2	DB01 DB00	I/O I/O	**External Memory Data Bus – Bit 01** **External Memory Data Bus – Bit 00**
A3	MGN	O	**Memory Output Enable** (Active low). Enables memory output on external memory data bus.
A4	MSN3	O	**Memory Select – Bit 3** (Active low). Selects byte 3 of memory addressed by the external memory address bus.
A5	MSN2	O	**Memory Select – Bit 2** (Active low). Selects byte 2 of memory addressed by the external memory address bus.
A6	MSN1	O	**Memory Select – Bit 1** (Active low). Selects byte 1 of memory addressed by the external memory address bus.
A7	MSN0	O	**Memory Select – Bit 0** (Active low). Selects byte 0 of memory addressed by the external memory address bus.

Table 23. Pin Descriptions by Alphanumerical Order — 13- x 13-Pin PGA Package (Continued)

Pin	Symbol	Type	Name/Description
A8	AB13	O	**External Memory Address Bus – Bit 13**
A9	AB12	O	**External Memory Address Bus – Bit 12**
A10	AB11	O	**External Memory Address Bus – Bit 11**
A11	AB09	O	**External Memory Address Bus – Bit 09**
A12	AB07	O	**External Memory Address Bus – Bit 07**
A13	AB06	O	**External Memory Address Bus – Bit 06**
B1	DB04	I/O	**External Memory Data Bus – Bit 04**
B2	DB03	I/O	**External Memory Data Bus – Bit 03**
B3	DB02	I/O	**External Memory Data Bus – Bit 02**
B4	MWN	O	**Memory Write** (Active low). Controls data writes to memory.
B5	VSS	P	**Ground**
B7	VDD	P	**+5 V**
B9	VSS	P	**Ground**
B10	AB10	O	**External Memory Address Bus – Bit 10**
B11	AB08	O	**External Memory Address Bus – Bit 08**
B12	AB05	O	**External Memory Address Bus – Bit 05**
B13	AB04	O	**External Memory Address Bus – Bit 04**
C1	DB06	I/O	**External Memory Data Bus – Bit 06**
C2	DB05	I/O	**External Memory Data Bus – Bit 05**
C3	VSS	P	**Ground**
C11	VSS	P	**Ground**
C12	AB03	O	**External Memory Address Bus – Bit 03**
C13	AB02	O	**External Memory Address Bus – Bit 02**
D1	DB09	I/O	**External Memory Data Bus – Bit 09**
D2	DB08	I/O	**External Memory Data Bus – Bit 08**
D3	DB07	I/O	**External Memory Data Bus – Bit 07**

Table 23. Pin Descriptions by Alphanumerical Order — 13- x 13-Pin PGA Package (Continued)

Pin	Symbol	Type	Name/Description
D11	CKI	I	**Clock In.** System clock.
D12	AB01	O	**External Memory Address Bus – Bit 01**
D13	AB00	O	**External Memory Address Bus – Bit 00**
E1	DB11	I/O	**External Memory Data Bus – Bit 11**
E2	DB10	I/O	**External Memory Data Bus – Bit 10**
E3	VDD	P	**+5 V**
E11	VDD	P	**+5 V**
E12	MMD0	I	**Memory Mode – Bit 0.** Decoded with MMD1 to select the address of on-chip memory. (See the Memory Addressing section.)
E13	MMD1	I	**Memory Mode – Bit 1.** Decoded with MMD0 to select the address of on-chip memory. (See the Memory Addressing section.)
F1	DB14	I/O	**External Memory Data Bus – Bit 14**
F2	DB13	I/O	**External Memory Data Bus – Bit 13**
F3	DB12	I/O	**External Memory Data Bus – Bit 12**
F11	CKO	O	**Clock Out.** Buffered clock at the same frequency as CKI. Synchronizes external devices to the DSP32.
F12	RESTN	I	**Reset** (Active low). Controls the DSP32 run/halt state. A high-to-low transition causes entry into the halt state. A low-to-high transition causes the reset sequence. Reset sequence stores PC in r14; clears PC, IOC, ESR, and sets EMR to mask all errors. The PCR register bits are cleared, except PCR0, which is set. CAU and DAU condition flags and the DAUC register are not affected by reset.
F13	ZN	I	**3-State** (Active low). When active, all DSP32 output pins are 3-stated. When not connected, ZN is inactive.
G1	DB16	I/O	**External Memory Data Bus – Bit 16**
G2	DB15	I/O	**External Memory Data Bus – Bit 15**
G3	VSS	P	**Ground**
G11	VSS	P	**Ground**
G12	PAB1	I	**Parallel Address Bus – Bit 1.** Bit 1 of 3-bit address from μP decoded along with PAB0 (pin H13) and PAB2 (pin G13) to select the lower or upper byte of PAR, PDR, or EMR. Also selects ESR/PCR.
G13	PAB2	I	**Parallel Address Bus – Bit 2.** Bit 2 of 3-bit address from μP decoded along with PAB0 (pin H13) and PAB1 (pin G12) to select the lower and upper byte of PAR, PDR, or EMR. Also selects ESR/PCR.
H1	DB19	I/O	**External Memory Data Bus – Bit 19**
H2	DB18	I/O	**External Memory Data Bus – Bit 18**
H3	DB17	I/O	**External Memory Data Bus – Bit 17**
H11	PWN	I	**Processor Write Enable** (Active low). When active, enables on-chip registers to be written by a μP.

Table 23. Pin Descriptions by Alphanumerical Order — 13- x 13-Pin PGA Package (Continued)

Pin	Symbol	Type	Name/Description
H12	PGN	I	**Processor Read Enable** (Active low). When active, enables PDB for output and allows the μP to read data from the selected PIO register.
H13	PAB0	I	**Parallel Address Bus – Bit 0.** Bit 0 of 3-bit address from μP decoded along with PAB1 (pin G12) and PAB2 (pin G13) to select the lower or upper byte of PAR, PDR, or EMR. Also selects ESR/PCR.
J1	DB21	I/O	**External Memory Data Bus – Bit 21**
J2	DB20	I/O	**External Memory Data Bus – Bit 20**
J3	V_{DD}	P	**+5 V**
J11	V_{DD}	P	**+5 V**
J12	PACK	I	**Processor Acknowledge.** Flag from μP acknowledging interrupt. PACK allows the μP to read PIR register and reset PINT.
J13	PEN	I	**Processor Interface Enable** (Active low). When active, enables read or write of the PIO data bus (PDB).
K1	DB24	I/O	**External Memory Data Bus – Bit 24**
K2	DB23	I/O	**External Memory Data Bus – Bit 23**
K3	DB22	I/O	**External Memory Data Bus – Bit 22**
K11	PDB2	I/O	**Parallel Data Bus – Bit 2**
K12	PDB1	I/O	**Parallel Data Bus – Bit 1**
K13	PDB0	I/O	**Parallel Data Bus – Bit 0**
L1	DB26	I/O	**External Memory Data Bus – Bit 26**
L2	DB25	I/O	**External Memory Data Bus – Bit 25**
L3	V_{SS}	P	**Ground**
L11	V_{SS}	P	**Ground**
L12	PDB4	I/O	**Parallel Data Bus – Bit 4**
L13	PDB3	I/O	**Parallel Data Bus – Bit 3**
M1	DB29	I/O	**External Memory Data Bus – Bit 29**
M2	DB28	I/O	**External Memory Data Bus – Bit 28**
M3	DB27	I/O	**External Memory Data Bus – Bit 27**
M4	DO	O	**Data Output.** Serial output PCM data. 3-stated when OEN is high.
M5	V_{SS}	P	**Ground**

Table 23. Pin Descriptions by Alphanumerical Order — 13- x 13-Pin PGA Package (Continued)

Pin	Symbol	Type	Name/Description
M6	SY	I/O	**Synchronization.** Internal Mode (Output) – DSP32 provides frame sync. External Mode (Input) – Frame sync is provided to the DSP32.
M7	V_{DD}	P	**+5 V**
M8	OCK	I/O	**Output Clock.** Clock for serial PCM output data. In internal mode, OCK is an output; in external mode, OCK is an input. (The mode is determined by the IOC register.)
M9	V_{SS}	P	**Ground**
M10	—	—	**Not used.** This pin must be left open.
M11	PDB7	I/O	**Parallel Data Bus – Bit 7**
M12	PDB6	I/O	**Parallel Data Bus – Bit 6**
M13	PDB5	I/O	**Parallel Data Bus – Bit 5**
N1	DB31	I/O	**External Memory Data Bus – Bit 31**
N2	DB30	I/O	**External Memory Data Bus – Bit 30**
N3	OEN	I	**Output Enable (Active low).** Enables DO for output. When high, DO is 3-stated.
N4	OSE	O	**Output Shift Register Empty.** Indicates end of serial transmission. The complement of OLD delayed by the number of bits in the transmission, as set by the IOC register.
N5	OBE	O	**Output Buffer Empty.** Indicates the state of serial PCM output buffer (OBUF). OBE is cleared when OBUF is written by the DSP32.
N6	IBF	O	**Input Buffer Full.** Indicates state of input buffer (IBUF). IBF is cleared when IBUF is loaded onto the data bus by DSP32.
N7	OLD	I/O	**Output Load.** Clock for loading parallel-to-serial converter from OBUF. In internal mode, OLD is an output; in external mode, OLD is an input. (The mode is determined by the IOC register.)
N8	ILD	I/O	**Input Load.** Clock for loading input buffer from serial-to-parallel converter. In internal mode, ILD is an output; in external mode, ILD is an input. (The mode is determined by the IOC register.)
N9	ICK	I/O	**Input Clock.** Clock for serial PCM input data. In internal mode, ICK is an output; in external mode, ICK is an input. (The mode is determined by the IOC register.)
N10	DI	I	**Data Input.** Serial PCM data into IBUF.
N11	—	—	**Not used.** This pin must be left open.
N12	PINT	O	**Processor Interrupt.** Interrupt to μP. PINT is set when a nonmasked error occurs or when the DSP32 writes to PIR and bit 2 of PCR is high. PINT is cleared by reading ESR or PIR, respectively.
N13	PDF	O	**Parallel Data Full.** Set when PDR is written by the DSP32 or a μP. PDR is cleared when PDR is read by the DSP32 or a μP.

Pins by Functional Group Order

Table 24. External Memory Interface Pins

Pin Number			Symbol	Type	Name/Description
40-pin	100-pin	13- x 13-pin			
—	D11	D13	AB00		External Memory Address Bus — Bit 00.
—	D10	D12	AB01		External Memory Address Bus — Bit 01.
—	C11	C13	AB02		External Memory Address Bus — Bit 02.
—	C10	C12	AB03		External Memory Address Bus — Bit 03.
—	B11	B13	AB04		External Memory Address Bus — Bit 04.
—	B10	B12	AB05		External Memory Address Bus — Bit 05.
—	A11	A13	AB06	O	External Memory Address Bus — Bit 06.
—	A10	A12	AB07		External Memory Address Bus — Bit 07.
—	D8	B11	AB08		External Memory Address Bus — Bit 08.
—	D7	A11	AB09		External Memory Address Bus — Bit 09.
—	C8	B10	AB10		External Memory Address Bus — Bit 10.
—	C7	A10	AB11		External Memory Address Bus — Bit 11.
—	B8	A9	AB12		External Memory Address Bus — Bit 12.
—	B7	A8	AB13		External Memory Address Bus — Bit 13.
—	A1	A2	DB00		External Memory Data Bus — Bit 00.
—	A2	A1	DB01		External Memory Data Bus — Bit 01.
—	B1	B3	DB02		External Memory Data Bus — Bit 02.
—	B2	B2	DB03		External Memory Data Bus — Bit 03.
—	C1	B1	DB04		External Memory Data Bus — Bit 04.
—	C2	C2	DB05		External Memory Data Bus — Bit 05.
—	D1	C1	DB06		External Memory Data Bus — Bit 06.
—	D2	D3	DB07		External Memory Data Bus — Bit 07.
—	E2	D2	DB08		External Memory Data Bus — Bit 08.
—	F1	D1	DB09		External Memory Data Bus — Bit 09.
—	F2	E2	DB10	I/O	External Memory Data Bus — Bit 10.
—	G1	E1	DB11		External Memory Data Bus — Bit 11.
—	G2	F3	DB12		External Memory Data Bus — Bit 12.
—	H1	F2	DB13		External Memory Data Bus — Bit 13.
—	H2	F1	DB14		External Memory Data Bus — Bit 14.
—	J1	G2	DB15		External Memory Data Bus — Bit 15.
—	J2	G1	DB16		External Memory Data Bus — Bit 16.
—	K1	H3	DB17		External Memory Data Bus — Bit 17.
—	K2	H2	DB18		External Memory Data Bus — Bit 18.
—	L1	H1	DB19		External Memory Data Bus — Bit 19.
—	L2	J2	DB20		External Memory Data Bus — Bit 20.
—	M1	J1	DB21		External Memory Data Bus — Bit 21.
—	M2	K3	DB22		External Memory Data Bus — Bit 22.

Table 24. External Memory Interface Pins (Continued)

Pin Number			Symbol	Type	Name/Description
40-pin	100-pin	13- x 13-pin			
—	N2	K2	DB23		**External Memory Data Bus — Bit 23.**
—	P1	K1	DB24		**External Memory Data Bus — Bit 24.**
—	P2	L2	DB25		**External Memory Data Bus — Bit 25.**
—	Q1	L1	DB26		**External Memory Data Bus — Bit 26.**
—	Q2	M3	DB27	I/O	**External Memory Data Bus — Bit 27.**
—	R1	M2	DB28		**External Memory Data Bus — Bit 28.**
—	R2	M1	DB29		**External Memory Data Bus — Bit 29.**
—	S1	N2	DB30		**External Memory Data Bus — Bit 30.**
—	S2	N1	DB31		**External Memory Data Bus — Bit 31.**
7	F11	E12	MMD0	I	**Memory Mode — Bit 0.**
8	F10	E13	MMD1		**Memory Mode — Bit 1.** MMD0 and MMD1 are decoded to select the address of on-chip memory (see the memory addressing section).
—	D4	A3	MGN	O	**Memory Output Enable (Active Low).** Enables memory output on external memory data bus.
—	D5	B4	MWN	O	**Memory Write (Active Low).** Controls data writes to memory.
—	A7	A7	MSN0		**Memory Select — Bit 0.**
—	A5	A6	MSN1	O	**Memory Select — Bit 1.**
—	B5	A5	MSN2		**Memory Select — Bit 2.**
—	B4	A4	MSN3		**Memory Select — Bit 3.** MSN0—MSN3 (active low), select individual bytes 0, 1, 2, or 3 of memory addressed by the external memory address bus.

Table 25. Parallel I/O Interface Pins

Pin Number			Symbol	Type	Name/Description
40-pin	100-pin	13- x 13-pin			
11	P11	K13	PDB0	I/O	**Parallel Data Bus — Bit 0.**
12	Q11	K12	PDB1		**Parallel Data Bus — Bit 1.**
13	Q10	K11	PDB2		**Parallel Data Bus — Bit 2.**
14	R11	L13	PDB3		**Parallel Data Bus — Bit 3.**
15	R10	L12	PDB4		**Parallel Data Bus — Bit 4.**
16	S11	M13	PDB5		**Parallel Data Bus — Bit 5.**
17	S10	M12	PDB6		**Parallel Data Bus — Bit 6.**
18	R8	M11	PDB7		**Parallel Data Bus — Bit 7.**
36	L11	H13	PAB0	I	**Processor Address Bus — Bit 0.**
35	L10	G12	PAB1		**Processor Address Bus — Bit 1.**
37	K11	G13	PAB2		**Processor Address Bus — Bit 2.** PAB0—PAB2 are decoded to select the lower or upper byte of PAR, PDR, or EMR. Also selects ESR/PCR.
32	P10	J12	PACK	I	**Processor Acknowledge.** Flag from μP acknowledging interrupt. PACK allows the μP to read PIR register and reset PINT.
33	N10	J13	PEN	I	**Processor Interface Enable (Active Low).** When active, PEN allows a read from or a write to the PIO data bus (PDB).
34	M11	H12	PGN	I	**Processor Read Enable (Active Low).** Allows μP to read data from the selected PIO register.
9	M10	H11	PWN	I	**Processor Write Enable (Active Low).** When active, enables on-chip registers to be written to by a μP.
19	Q8	N12	PINT	O	**Processor Interrupt.** Interrupt to μP. PINT is set when a nonmasked error occurs, or when the DSP32 writes to PIR and bit 2 of PCR is set; PINT is cleared by reading ESR or PIR.
20	P8	N13	PDF	O	**Parallel Data Full.** Set when PDR is written to by the DSP32 or a μP; cleared when PDR is read by the DSP32 or by a μP.

Table 26. Serial I/O Interface Pins

Pin Number			Symbol	Type	Name/Description
40-pin	100-pin	13- x 13-pin			
31	P7	N10	DI	I	**Data Input.** Serial PCM data in to IBUF.
29	Q5	N6	IBF	O	**Input Buffer Full.** Indicates state of input buffer (IBUF). IBF is cleared when IBUF is loaded onto the data bus by DSP32.
30	R7	N9	ICK	I/O	**Input Clock.** Clock for serial PCM input data. In internal mode ICK is an output; in external mode ICK is an input, depending on the I/O format.
28	Q7	N8	ILD	I/O	**Input Load.** Clock for loading input buffer from serial-to-parallel converter. In internal mode ILD is an output; in external mode ILD is an input, depending on the I/O format.
23	Q4	M4	DO	O	**Data Output.** Serial PCM data output from OBUF. 3-stated when OEN is set.
22	P5	N5	OBE	O	**Output Buffer Empty.** Indicates the state of serial PCM output buffer (OBUF). OBE is cleared when OBUF is written to by the DSP32.
21	S7	M8	OCK	I/O	**Output Clock.** Clock for serial PCM output data. In internal mode OCK is an output; in external mode OCK is an input, depending on the I/O format.
24	S5	N7	OLD	I/O	**Output Load.** Clock for loading parallel-to-serial converter from OBUF. In internal mode OLD is an output; in external mode OLD is an input, depending on the I/O format.
25	R4	N4	OSE	O	**Output Shift Register Empty.** Indicates end of serial transmission. Complement of OLD. Delayed by the number of bits in the transmission as set by the IOC register.
26	P4	N3	OEN	I	**Output Enable (Active Low).** Enables DO for output. When high, DO is 3-stated.
27	R5	M6	SY	I/O	**Synchronization.** In internal mode (output), DSP32 provides frame sync; in external mode (input), frame sync is provided to the DSP32.

Table 27. Utility, Power, and Ground Pins

Pin Number			Symbol	Type	Name/Description
40-pin	100-pin	13- x 13-pin			
5	E10	D11	CKI	I	**Clock In.** Input clock.
4	H11	F11	CKO	O	**Clock Out.** Buffered clock at the same frequency as CKI. Synchronizes external devices to the DSP32.
10	G10	F12	RESTN	I	**Reset (Active Low).** Controls the DSP32 run/halt state. A high-to-low transition causes entry into the halt state; a low-to-high transition causes the reset sequence. Reset sequence stores PC in r14; clears PC, IOC, ESR; and sets EMR to mask all errors. The PCR register bits, except PCR0, are cleared; PCR0 is set. CAU and DAU condition flags and the DAUC registers are to affected by reset.
6	G11	F13	ZN	I	**3-State (Active Low).** When active, all DSP32 output pins are 3-stated; when not connected, ZN is inactive.
—	E1 N1	—	VDD	P	**5 V Supply.** For external memory interface. If external memory is not used, this pin must be connected to VSS.
38 39 40	E11 N11	B7, E3, E11, J3, J11, M7	VDD	P	**5 V Supply.**
1 2 3	A4 A8 J11 S4 S8	B5, B9, C3, C11, G3, G11, L3, L11, M5, M9	VSS	P	**Ground.**
—	C4 C5 H10 J10 K10	M10 N11	—	—	**Not Used.** These pins must be left open.

Characteristics

Electrical Characteristics and Requirements

The parameters below are valid for the following conditions: T_C = 0 to 115 °C; V_{SS} = 0 V.

Table 28. Input and Output Parameters

Parameter	Sym	16 MHz			25 MHz			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply voltage	V_{DD}	4.5	5.0	5.5	4.75	5.0	5.25	V
Input voltage:								
All inputs except ZN								
low	V_{IL}	—	—	0.8	—	—	0.8	V
high	V_{IH}	2.4	—	—	2.4	—	—	V
ZN								
low	V_{IL}	—	—	V_{SS}	—	—	V_{SS}	V
high	V_{IH}	Open	—	—	Open	—	—	V
Output voltage:								
low (I_{OL} = 2 mA)	V_{OL}	—	—	0.4	—	—	0.4	V
high (I_{OH} = –0.2 mA)	V_{OH}	2.4	—	—	2.4	—	—	V
Input leakage:								
All inputs except ZN								
low (V_{IL} = 0 V)	I_{IL}	–10	—	—	–10	—	—	μA
high (V_{IH} = V_{DD} max)	I_{IH}	—	—	10	—	—	10	μA
ZN								
low (V_{IL} = 0 V)	I_{IL}	–500	—	—	–500	—	—	μA
high (V_{IH} = V_{DD} max)	I_{IH}	—	—	20	—	—	20	μA
Input capacitance	C_I	—	—	10	—	—	10	pF
Output offset current:								
low (V_{OL} = 0 V)	I_{OZL}	–20	—	—	–20	—	—	μA
high (V_{OH} = V_{DD} max)	I_{OZH}	—	—	20	—	—	20	μA

Table 28. Input and Output Parameters (Continued)

Parameter	Sym	16 MHz			25 MHz			Unit
		Min	Typ	Max	Min	Typ	Max	
Power supply current:	IDD							
TC = 0 °C								
40-pin package		—	—	550	—	—	570	mA
100-pin package without EMI*		—	—	550	—	—	570	mA
100-pin package with EMI*		—	—	600	—	—	630	mA
13- x 13-pin package		—	—	600	—	—	630	mA
TC = 115 °C								
40-pin package		—	360	420	—	420	440	mA
100-pin package without EMI*		—	360	420	—	420	440	mA
100-pin package with EMI*		—	400	470	—	470	495	mA
13- x 13-pin package		—	400	470	—	470	495	mA
Power dissipation:	PD							
TC = 0 °C								
40-pin package		—	—	3.0	—	—	3.0	W
100-pin package without EMI*		—	—	3.0	—	—	3.0	W
100-pin package with EMI*		—	—	3.3	—	—	3.3	W
13- x 13-pin package		—	—	3.3	—	—	3.3	W
TC = 115 °C								
40-pin package		—	1.8	2.3	—	2.1	2.3	W
100-pin package without EMI*		—	1.8	2.3	—	2.1	2.3	W
100-pin package with EMI*		—	2.0	2.6	—	2.3	2.6	W
13- x 13-pin package		—	2.0	2.6	—	2.3	2.6	W

* EMI = external memory interface.

Output Drive

The DSP32 device drives into 50 pF with currents of +2.0 mA I_{OL} and –200 μA I_{OH} and still maintains output voltages of 0.4 V (max) V_{OL} and 2.4 V (min) V_{OH}.

RAM Hold Time

The DSP32 device includes an internal mechanism for automatic refresh of the internal RAM. This refresh is always enabled when the device is reset. It consumes 4 periods of CKI every 128 periods, or about 3% of the DSP32 instruction execution time. The refresh can be disabled by setting bit 7 of the PCR register. This is accomplished by using the PIO port subsequent to the reset. If the refresh is disabled, the RAM hold time is guaranteed to be a minimum of 4 ms.

Absolute Maximum Ratings

Maximum ratings are the limiting conditions that can be applied under all variations of circuit and environmental conditions without the occurrence of permanent damage.

Voltage on any pin with respect to ground ..... –0.5 to +6.5 V
Storage temperature range ..... –65 to +150 °C

Warning: To avoid excessive power supply current, power should not be supplied to V_{DD} when CKI is not active.

Ambient Temperature

The allowable ambient temperature, TA, in °C can be obtained from the following formula:

$$T_A = T_C - (PD \times \theta_{CA})$$

Where:

TC	=	Chip case temperature, °C
PD	=	Power dissipation, W
θ_{CA}	=	Thermal resistance, case-to-ambient, °C/W

The maximum ambient temperature for various arrangements with no air flow is given below.

Package Option	PD (W)	θ_{CA} (°C/W)	TA (°C)
100-pin PGA:			
with EMI	2.6	19	65
without EMI	2.3	19	71
13- x 13-Pin PGA	2.6	19	65
40-pin DIP:			
no heat sink	2.3	32	41
Aavid 6107 heat sink	2.3	23	62

The maximum allowable ambient temperature can be increased with the use of air flow. The thermal resistance as a factor of air flow is shown in Figure 7. The minimum air flow required for an ambient temperature of 70°C for various package options is shown below.

Package Option	PD (W)	Air Flow (Ft./Min.)
100-pin PGA:		
with EMI	2.6	80
without EMI	2.3	0
13- x 13-Pin PGA	2.6	80
40-pin DIP:		
no heat sink	2.3	370
Aavid 5807 heat sink	2.3	70

Handling Precautions

All MOS devices must be handled with certain precautions in order to avoid damage due to the accumulation of static charge. Although input protection circuitry has been incorporated into the devices to minimize the effect of this static buildup, proper precautions should be taken to avoid exposure to electrostatic discharge during handling and mounting. AT&T employs a human body model and a charged device model for ESD susceptibility testing. Since the failure voltage of electronic devices is dependent on the current and voltage and, hence, the resistance and capacitance, it is important that standard values are employed to establish a reference by which to compare test data. Values of 100 pF and 1500 Ω are the most common and are the values used in the AT&T human body model test circuit. The breakdown voltage for the DSP32 device is 900 V, according to the human body model. Test data for the charged device model is available upon request.

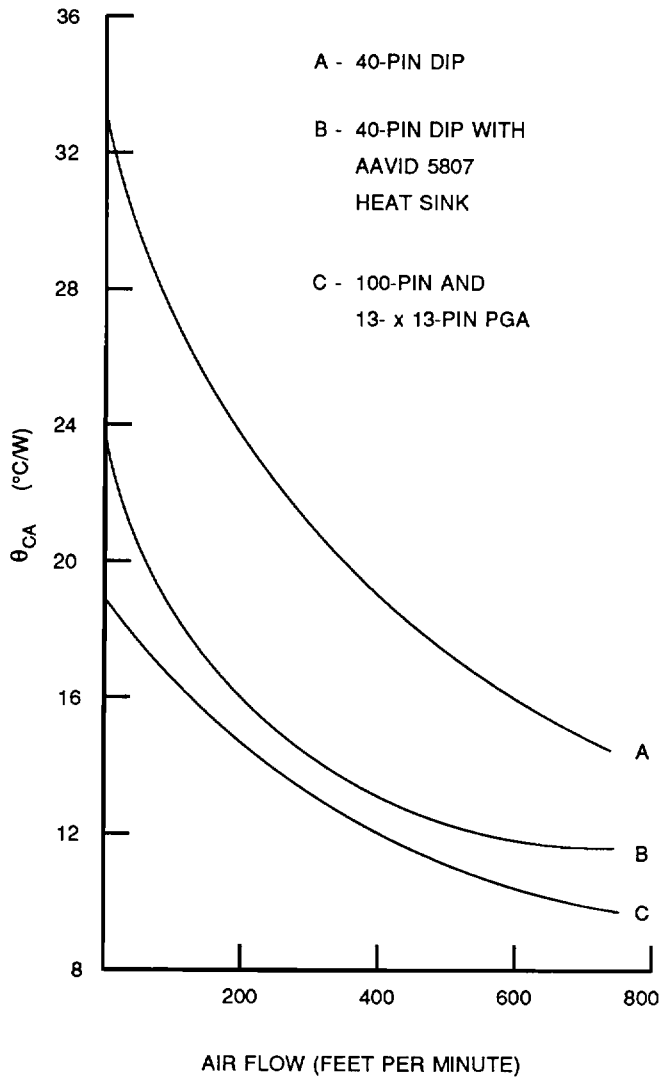


Figure 7. Thermal Resistance

Timing Characteristics and Requirements

Device Timing Characteristics and Requirements

V_{DD} = 5 V ± 10% (for 16-MHz part); V_{DD} = 5 V ± 5% (for 25-MHz part); V_{SS} = 0 V; T_C = 0 to 115 °C; C_{LOAD} = 50 pF

Table 29. Timing Requirements for Clocks (See Figure 8)

Description	Symbol	16 MHz		25 MHz		Unit
		Min	Max	Min	Max	
Clock in period	tCKILCKIL	61	125	40	125	ns
Clock in low time	tCKILCKIH	27.5	—	18	—	ns
Clock in high time	tCKIHCKIL	27.5	—	18	—	ns

The timing characteristics and requirements for the external memory interfaces of the 16-MHz and 25-MHz parts are specified in different manners. The timing characteristics and specifications for the 16-MHz part are shown in Tables 30—32. The timing characteristics and specifications for the 25-MHz part are shown in Tables 33—35.

Table 30. Direct Timing Characteristics for External Memory Interface (16-MHz Only)

Description	Symbol	Min	Max	Unit	Fig
MGN low delay	tCKILMGNL	10	45	ns	9
MGN high delay	tCKILMGNH	10	45	ns	9
MWN low delay	tCKIHMWNL	15	50	ns	10
MWN high delay	tCKIHMWNH	15	50	ns	10
Clock out low delay	tCKILCKOL	20	55	ns	8
Clock out high delay	tCKIHCKOH	20	55	ns	8
Address valid delay	tCKILAV	20	55	ns	—
Address valid hold	tCKILAX	15	40	ns	—
Data out valid delay	tCKIHDV	—	50	ns	—
Data out hold*	tCKILDZ	30	55	ns	—

* The Z-state termination point is defined as a change of 0.5 V with a load of ± 2 mA.

Table 31. Timing Characteristics for External Memory Interface (16-MHz Only)

Description	Symbol	Min*	Max*	Unit	Fig
Address valid	tAVAX	2T – 20	—	ns	11
Address set-up to read	tAVGL	T – 15	T	ns	11
Address valid to end of read	tAVGH	2T – 15	2T	ns	11
Width of read strobe	tGLGH	T – 10	T + 10	ns	11
Address set-up to write	tAVWL	θL – 25	θL	ns	12
Address valid to end of write	tAVWX	T + θL – 25	T + θL	ns	12
Data set-up to write	tDVWH	T – 25	—	ns	12
Data hold after write**	tWHDZ	θH	—	ns	12
Width of write strobe	tWLWH	T – 10	T + 10	ns	12

* T = tCKILCKIL; θL = tCKILCKIH; θH = tCKIHCKIL.
** The Z-state termination point is defined as a change of 0.5 V with a load of ± 2 mA.

Table 32. Timing Requirements for External Memory Interface (16-MHz Only)

Description	Symbol	Min	Max*	Unit	Fig
Address access	tAVDV	—	2T – 40	ns	11
Data enable	tGLDV	—	T – 20	ns	11
Data set-up	tDVGH	10	—	ns	11
Data disable	tGHDZ	0	θL	ns	11

* T = tCKILCKIL; θL = tCKILCKIH; θH = tCKIHCKIL.

Table 33. Direct Timing Characteristics for External Memory (25-MHz Only)

Description	Symbol	Min	Max	Unit	Fig
MGN low delay	tCKILMGNL	—	35	ns	9
MGN high delay	tCKILMGNH	—	40	ns	9
MWN low delay	tCKIHMWNL	—	40	ns	10
MWN high delay	tCKIHMWNH	—	40	ns	10

Table 34. Timing Characteristics for External Memory (25-MHz Only)

Description	Symbol	Min*	Max*	Unit	Figure
Address set-up to read	tAVGL	T – 15	—	ns	13
Address hold after read	tGHAX	– 15	—	ns	13
Width of read strobe	tGLGH	T – 10	—	ns	13
Address set-up to write	tAVWL	θL – 17	—	ns	14
Address hold after write	tWHAX	0	—	ns	14
Data set-up to write	tDVWH	T – 20	—	ns	14
Data hold after write**	tWHDZ	θH	θH + 20	ns	14
Width of write strobe	tWLWH	T – 10	—	ns	14

* T = tCKILCKIL; θL = tCKILCKIH; θH = tCKIHCKIL.
** The Z-state termination point is defined as a change of 0.5 V with load of ± 2 mA.

Table 35. Timing Requirements for External Memory (25-MHz Only)

Description	Symbol	Min	Max*	Unit	Figure
Address access	tAVDV	—	2T – 30	ns	13
Data enable	tGLDV	—	T – 17	ns	13
Data set-up	tDVGH	10	—	ns	13
Data hold	tGHDX	–10	—	ns	13
Data disable	tGHDZ	—	θL	ns	13

* T = tCKILCKIL; θL = tCKILCKIH; θH = tCKIHCKIL.

Summary of Timing Characteristics for External Memory Interface

To assist in selecting memory devices, the following table summarizes the ac characteristics that must be met by memory devices connected to the DSP32 memory interface.

Table 36. Timing Characteristics for External Memory Interface

Description	16 MHz*	25 MHz*
Read cycle:		
Read cycle time tAVAX	2T – 20 102 ns (min)	2T – 17 63 ns (min)
Address valid to data valid tAVDV	2T – 40 82 ns (max)	2T – 30 50 ns (max)
Chip select**	2T – 40 82 ns (max)	2T – 30 50 ns (max)
Read pulse width tGLGH	T – 10 51 ns (max)	T – 10 30 ns (max)
Output enable low to output valid tGLDV	T – 20 41 ns (max)	T – 17 23 ns (max)
Output enable high to output high Z (hold time) tGHDZ	θL 27.5 ns (max)	θL 18 ns (max)
Write cycle ($\overline{W}$ controlled):		
Write cycle time tAVAX	2T – 20 102 ns (min)	2T – 17 63 ns (min)
Address valid to end of write tAVWX	T + θL – 25 63.5 ns (min)	T + θL – 17 41 ns (min)
Write pulse width tWLWH	T – 10 51 ns (min)	T – 10 30 ns (min)
Data valid to end of write tDVWH	T – 25 36 ns (min)	T – 20 20 ns (min)
Data hold time	θH 27.5 ns (min)	θH 18 ns (min)

* T = tCKILCKIL (clock in period).
θL = tCKILCKIH (clock in low time).
θH = tCKIHCKIL (clock in high time).
** Same as address access time, assuming MSN0—MSN3 are connected to CS.

Table 37. Timing Requirements for Serial Inputs (See Figure 15)

Description	Symbol	16 MHz		25 MHz		Unit
		Min	Max	Min	Max	
Clock period	tICKLICKL	122	1000	80	1000	ns
Clock low time	tICKLICKH	50	—	35	—	ns
Clock high time	tICKHICKL	50	—	35	—	ns
Load high set-up	tILDHICKH	40	—	25	—	ns
Load high hold	tICKHILDL	0	—	0	—	ns
Load low set-up	tILDLICKH	40	—	25	—	ns
Load low hold	tICKHILDH	0	—	0	—	ns
Data set-up	tDIVICKH	35	—	25	—	ns
Data hold	tICKHDIX	0	—	0	—	ns

Table 38. Timing Characteristics for Serial Input (See Figure 15)

Description	Symbol	16 MHz		25 MHz		Unit
		Min	Max	Min	Max	
Input buffer delay	tICKHIBFH	—	75	—	50	ns

Table 39. Timing Requirements for Serial Output (See Figure 16)

Description	Symbol	16 MHz		25 MHz		Unit
		Min	Max	Min	Max	
Clock period	tOCKLOCKL	122	1000	80	1000	ns
Clock low time	tOCKLOCKH	50	—	35	—	ns
Clock high time	tOCKHOCKL	50	—	35	—	ns
Load high set-up	tOLDHOCKH	40	—	25	—	ns
Load high hold	tOCKHOLDL	0	—	0	—	ns
Load low set-up	tOLDLOCKH	40	—	25	—	ns
Load low hold	tOCKHOLDH	0	—	0	—	ns

Table 40. Timing Characteristics for Serial Output (See Figure 16)

Description	Symbol	16 MHz		25 MHz		Unit
		Min	Max	Min	Max	
Data delay	tOCKHDOV	—	50	—	35	ns
Data hold	tOCKHDOX	5	—	3	—	ns
Output buffer empty delay	tOCKHOBEH	—	75	—	50	ns
Output shift register delay	tOCKHOSEH	—	75	—	50	ns
Enable delay	tOENLDOV	—	100	—	65	ns
Disable delay*	tOENHDOZ	—	100	—	65	ns

* The Z-state termination point is defined as a change of 0.5 V with a load of ± 2 mA.

Serial I/O (SIO) Timing Characteristics and Requirements

Table 41. Timing Requirements for Serial Clock Generation* (See Figure 17a)

Description	Symbol	16 MHz		25 MHz		Unit
		Min	Max	Min	Max	
SY high set-up	tSYHICKH tSYHOCKH	35	—	25	—	ns
SY high hold	tICKHSYL tOCKHSYL	0	—	0	—	ns
SY low set-up	tSYLICKH tSYLOCKH	35	—	25	—	ns
SY low hold	tICKHSYH tOCKHSYH	0	—	0	—	ns

* ICK or OCK is selected by IOC[BC].

Table 42. Timing Characteristics for Serial Clock Generation (See Figures 17a, b, and c)

Description	Symbol	16 MHz		25 MHz		Unit	Fig
		Min	Max	Min	Max		
Internal SY delay*	tICKHSYL tOCKHSYL	—	75	—	50	ns	17b
Internal load delay*	tICKHILDL tOCKHOLDL	—	85	—	60	ns	17b
Internal load/SY delay	tSYLILDL tSYLOLDL	—	50	—	35	ns	17a
Clock period**	tICKHICKH tOCKHOCKH	488	1000	320	1000	ns	17c
Clock low time	tICKLICKH tOCKLOCKH	220	—	144	—	ns	17c
Clock high time	tICKHICKL tOCKHOCKL	220	—	144	—	ns	17c

* ICK or OCK is selected by IOC[BC].
** tICKHICKH and tOCKHOCKH are tCKIHCKIH * 8.

Parallel I/O (PIO) Timing Characteristics and Requirements

Table 43. Timing Requirements for PIO Read Cycle* (See Figure 18)

Description	Symbol	16 MHz		25 MHz		Unit
		Min	Max	Min	Max	
Address set-up	tPAVPRL	25	—	15	—	ns
PACK set-up	tPACKHPRL	25	—	15	—	ns
Address hold	tPRHPAX	0	—	0	—	ns
PACK hold	tPRHPACKL	0	—	0	—	ns

* For the 16-MHz device, a minimum 200-ns interval is required before the start of a read or write cycle following the end of the previous read or write cycle. For the 25-MHz device, a 120-ns interval is required.

Table 44. Timing Characteristics for PIO Read Cycle (See Figure 18)

Description	Symbol	16 MHz		25 MHz		Unit
		Min	Max	Min	Max	
Access from read*	tPRLPDV	—	100	—	65	ns
Data hold from read	tPRHPDZ	5	70	—	50	ns

* Read access time is for 150-pF loading on the PDB. With 200-pF loading, the maximum read access time is 130 ns.

Table 45. Timing Requirements for PIO Write Cycle* (See Figure 19)

Description	Symbol	16 MHz		25 MHz		Unit
		Min	Max	Min	Max	
Address set-up	tPAVPWL	25	—	15	—	ns
Address hold	tPWHPAX	0	—	0	—	ns
Write pulse	tPWLPWH	80	—	55	—	ns
Data set-up	tPDVPWH	50	—	35	—	ns
Data hold	tPWHPDX	0	—	0	—	ns

* For the 16-MHz device, a minimum 200-ns interval is required before the start of a read or write cycle following the end of the previous read or write cycle. For the 25-MHz device, a 120-ns interval is required.

Table 46. Timing Characteristics for PDF and PINT (See Figures 18 and 19)

Description	Symbol	16 MHz		25 MHz		Unit
		Min	Max	Min	Max	
PDF write delay	tPWHPDFH	—	120	—	85	ns
PDF read delay	tPRLPDFL	—	120	—	85	ns
PINT read delay	tPRLPINTL	—	150	—	105	ns
PINT read delay	tPRHPINTL	—	150	—	105	ns

Reset Timing Characteristics and Requirements

When the DSP32 device is powered-up, the dynamic RAM access strobes must be established before internal RAM accesses can be guaranteed. This can be accomplished in one of two ways. If the RAM autorefresh is enabled for a sufficient length of time (512 X tCKILCKIL) before the first internal RAM access, the refresh mechanism establishes the access strobes; otherwise, it is recommended that the DSP32 application program perform four dummy reads of each 512-word bank of internal RAM to establish the access strobes. This recommendation also applies to applications where PIO DMA transfers to internal DSP32 RAM occur after reset.

The DSP32 device can be reset and halted by using either the PCR register or the RESTN pin. The PCR register is externally controlled through the PIO port.

Reset Using the PCR Register. With the RESTN input high, the DSP32 device is halted by writing PCR0 = 0. It must remain halted for at least 22 periods of CKI (T). To bring the device out of halt and then begin execution, set PCR = 0x80, followed by PCR = 0x81. The other PCR bits can be set or cleared according to the application requirements. The timing requirements for the PCR writes are provided in Figure 19.

Reset Using the RESTN Pin. The sequence required to initialize and run the DSP32 device is shown in Figure 20. The first low-to-high transition is required to initialize internal DSP32 registers. The next transition causes the DSP32 to begin execution. The valid address (all low) to the first instruction appears on the external address bus after the time interval. Note that, if the device is reset by using RESTN, the PCR0 = 0 half is overridden and PCR0 is set (PCR1—PCR7 are cleared) after the first low-to-high transition of RESTN. SIO DMA can not be enabled during the first four instruction cycles.

At any time after the initial power-up sequence, the device can be halted by a high-to-low transition of RESTN (see Figure 21). If the user wishes all instructions in the progress to execute to completion, the DSP32 must remain halted for at least 22 periods of CKI(T). The PIO port and the internal RAM refresh mechanism are active during halt. After halt, a single low-to-high transition of RESTN is sufficient to restart the DSP32 device at the first instruction.

Table 47. Reset Timing Requirements and Characteristics for RESTN (See Figures 20 and 21)

Description	Symbol	16 MHz		25 MHz		Unit
		Min	Max	Min	Max	
RESTN low set-up	tRSTLCKIH	0	θL	0	θL	ns
RESTN high set-up	tRSTHCKIH	0	θL	0	θL	ns
Interval to PC = 0	tSTART	7T + 20	7T + 55	7T + 13	7T + 37	ns
First RESTN low	tRLOW1	T	—	T	—	ns
First RESTN high	tRHIGH1	T	4T	T	4T	ns
Second RESTN low	tROWL2	22T	100T	22T	100T	ns

* T = tCKILCKIL; θL = tCKILCKIH; θH = tCKIHCKIL.

Timing Diagrams

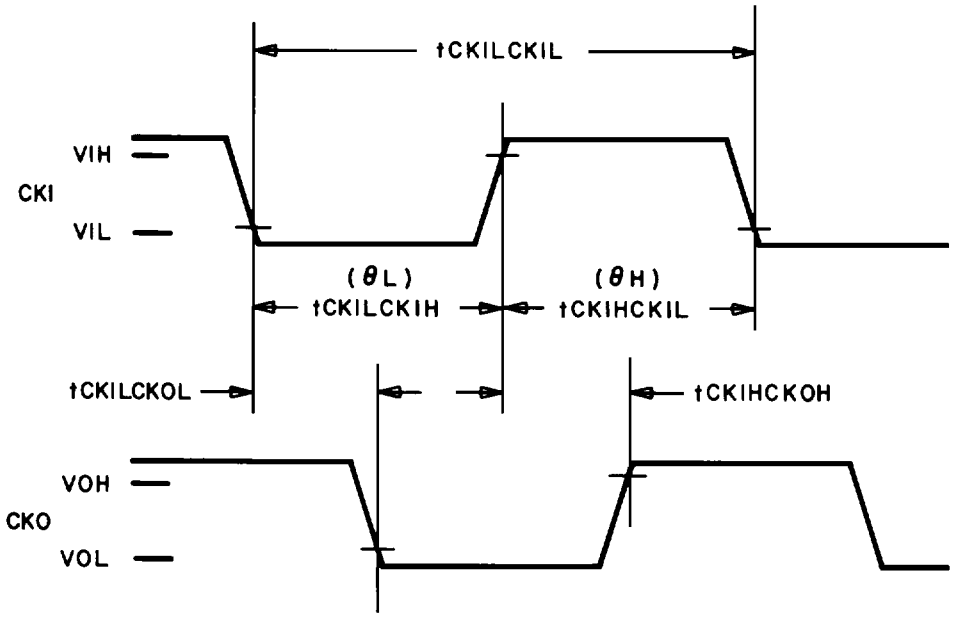


Figure 8. Clocks

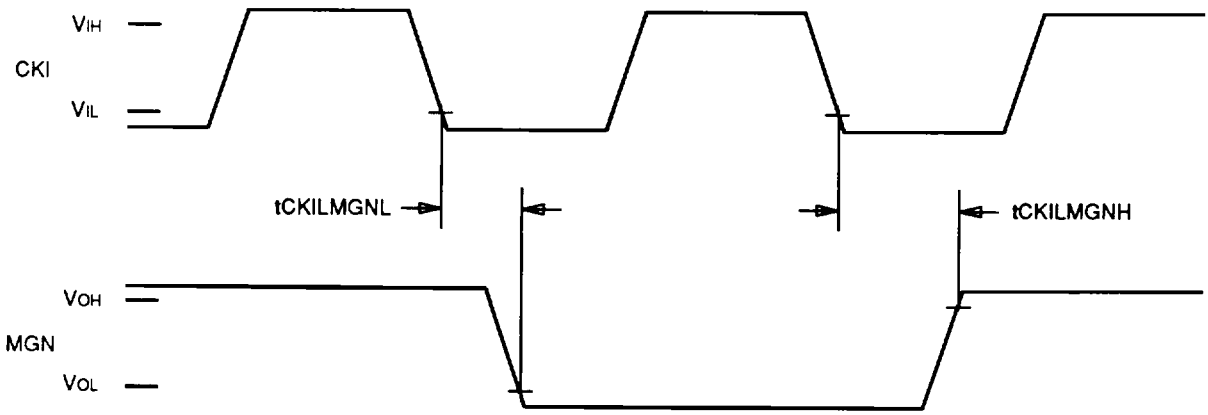


Figure 9. MGN Direct Timing

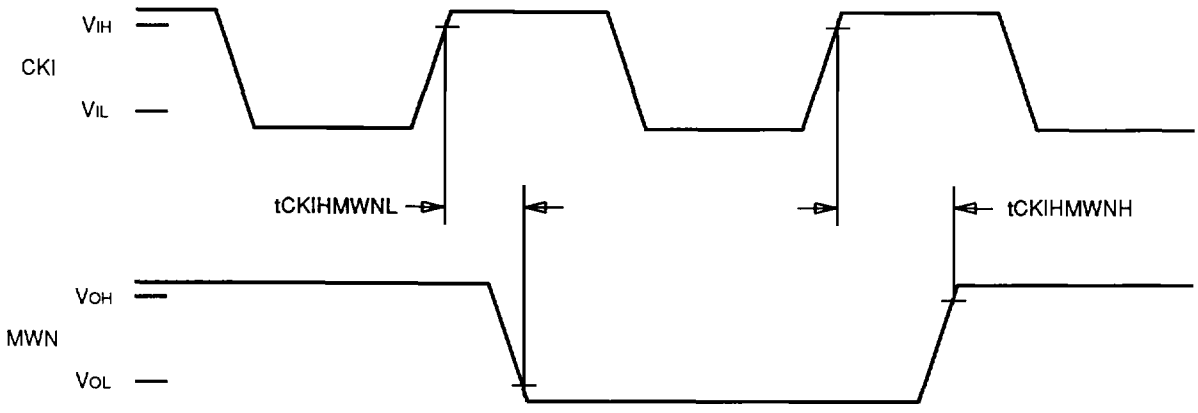


Figure 10. MWN Direct Timing

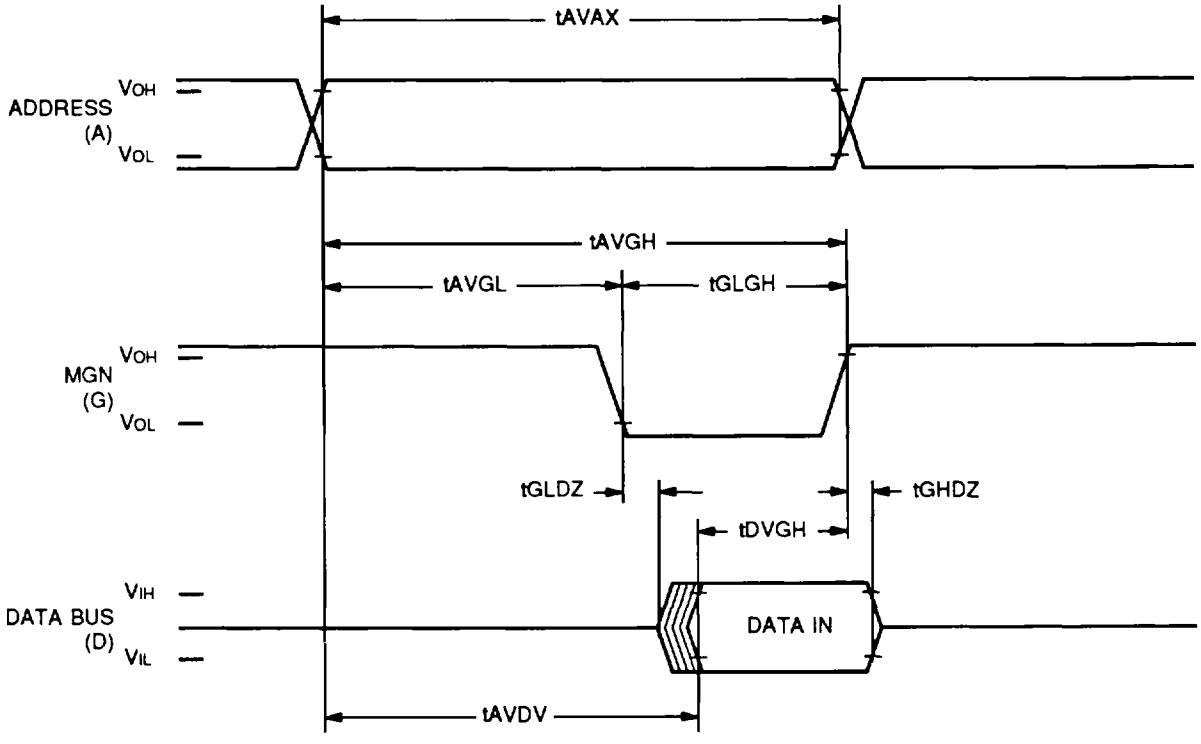


Figure 11. External Memory Read Cycle for 16-MHz Device

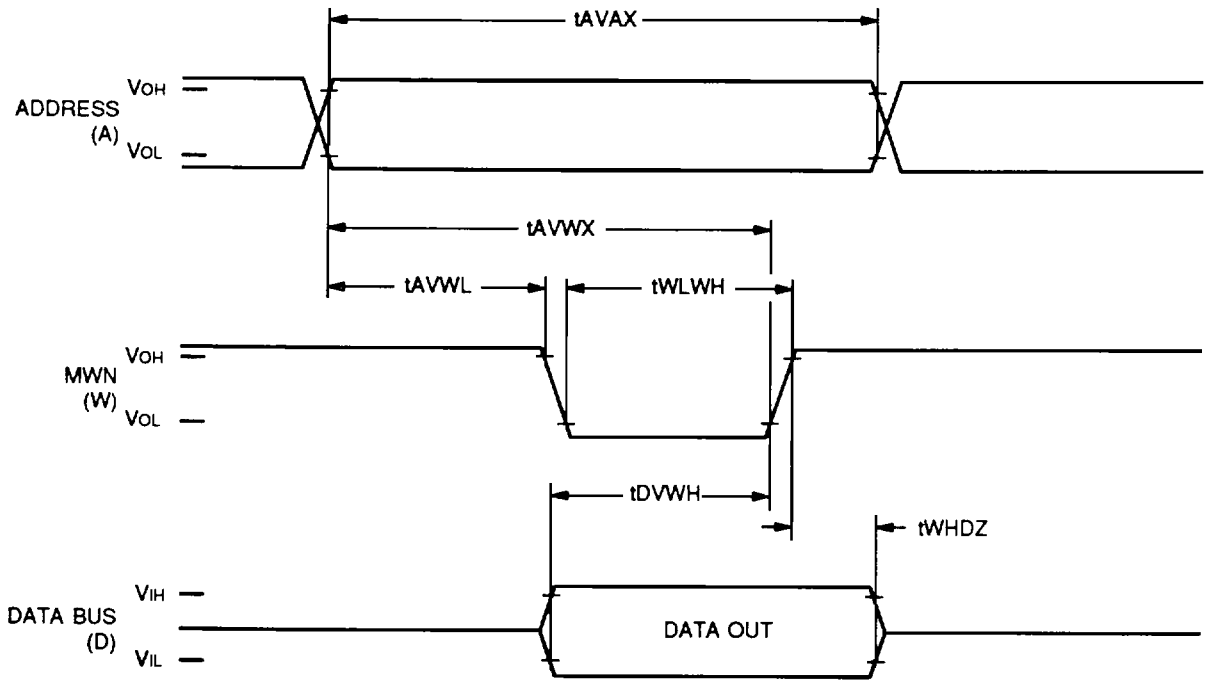


Figure 12. External Memory Write Cycle for 16-MHz Device

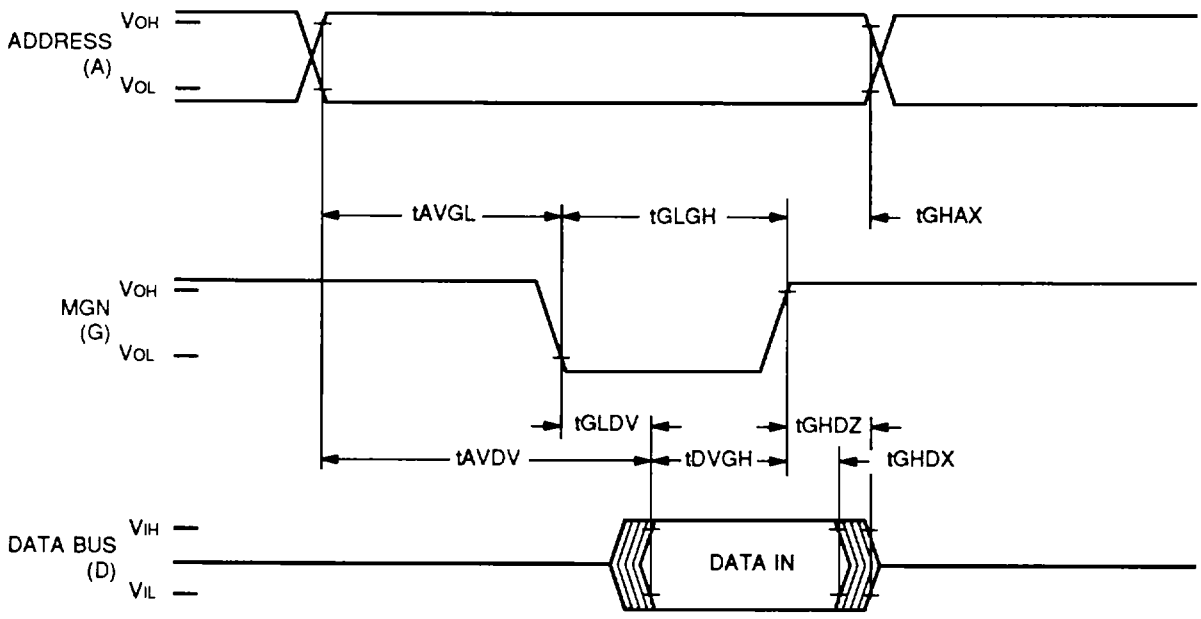


Figure 13. External Memory Read Cycle for 25-MHz Device

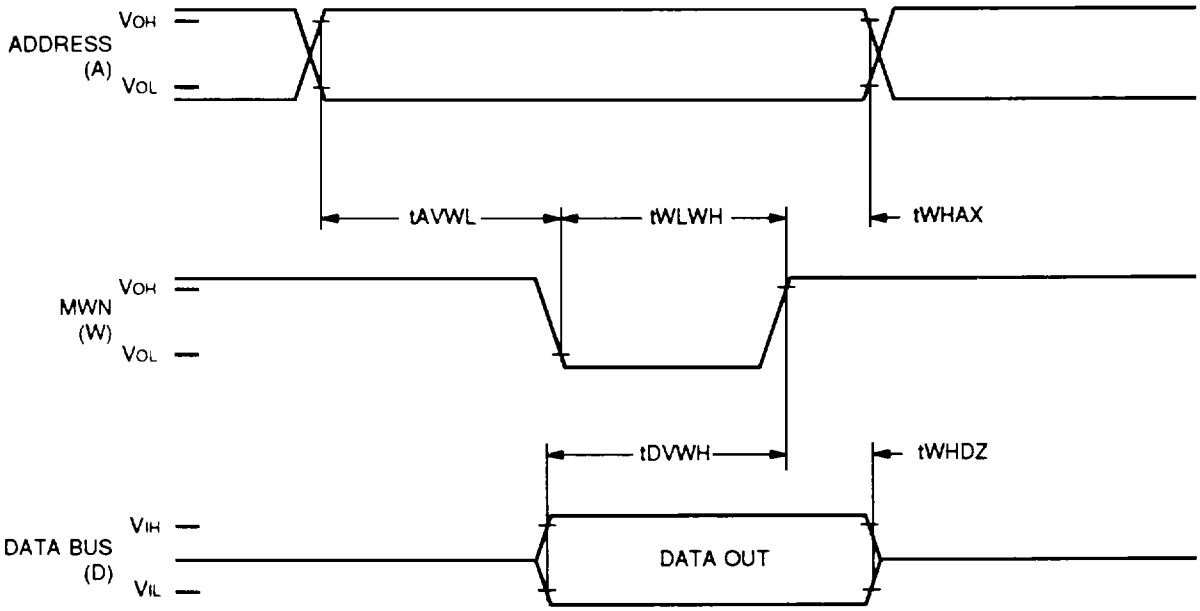


Figure 14. External Memory Write Cycle for 25-MHz Device

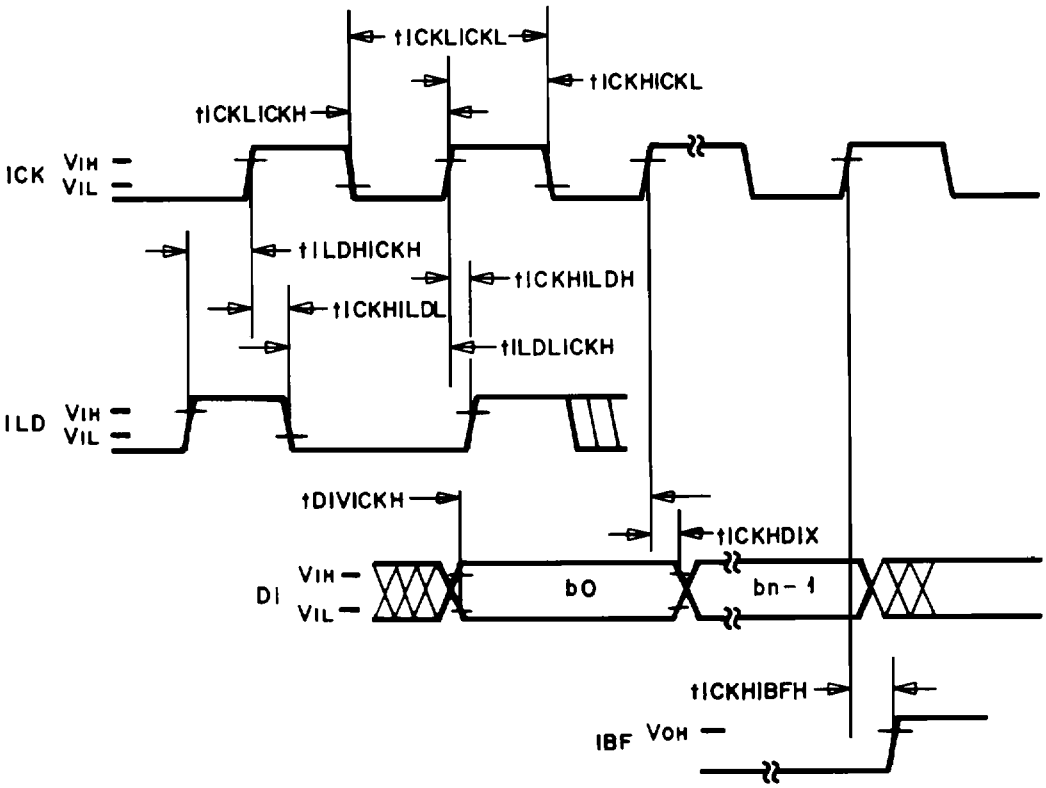


Figure 15. Serial Input Timing

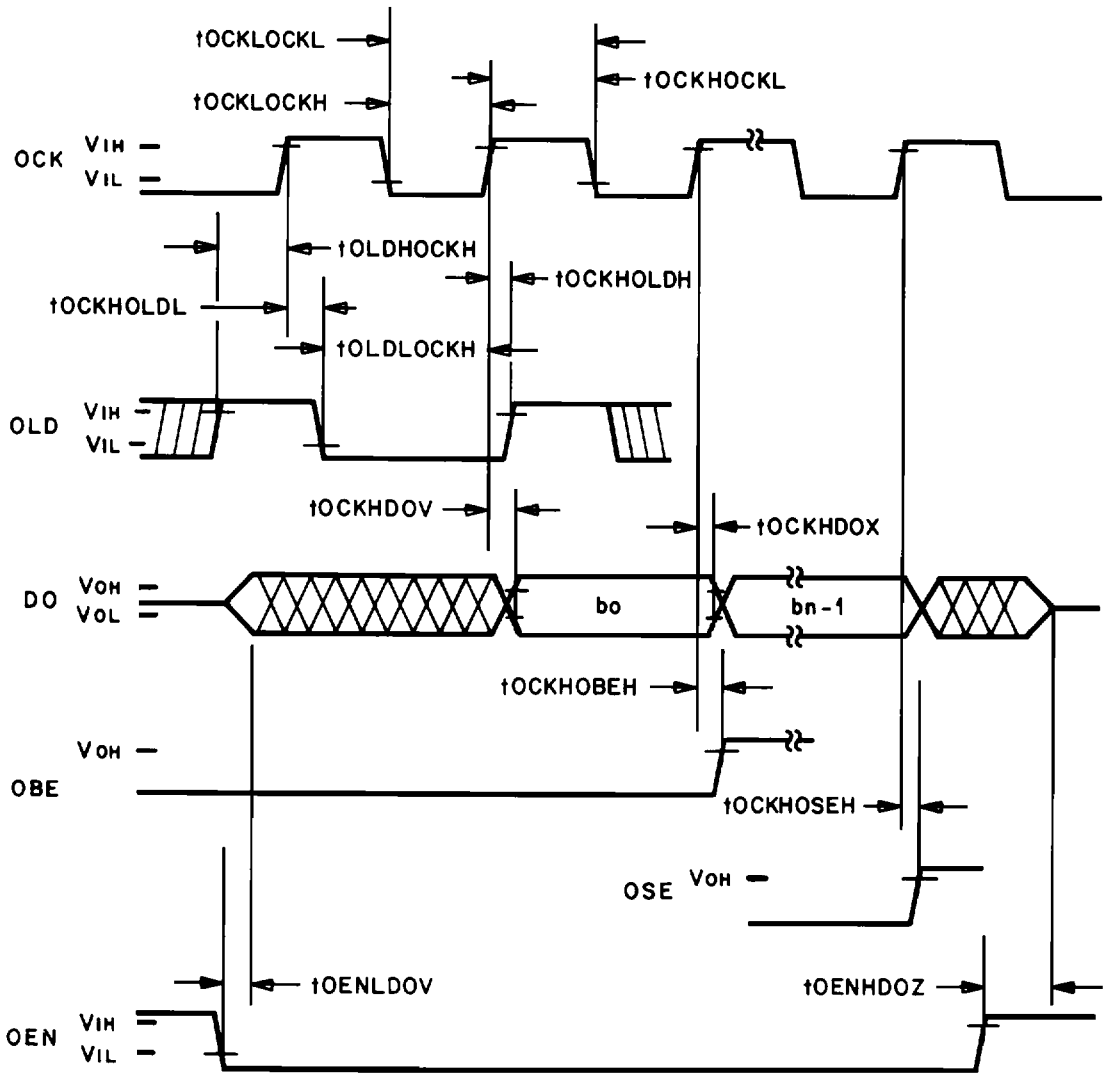
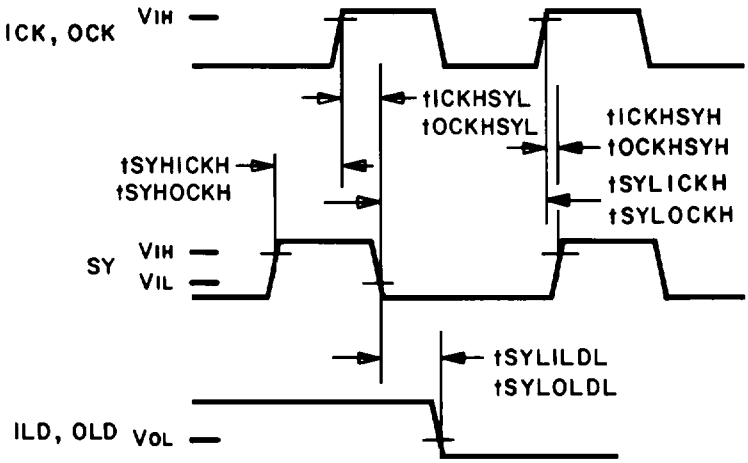
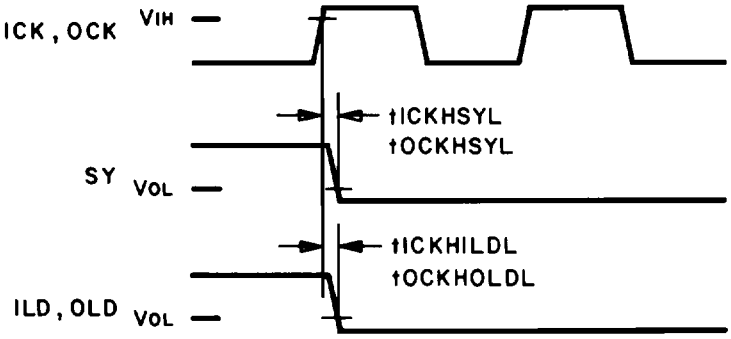


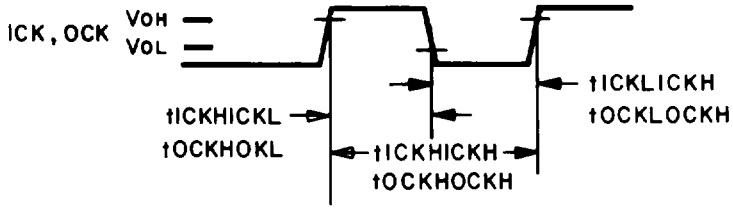
Figure 16. Serial Output Timing



(a) EXTERNAL SY, ICK/OCK. INTERNAL ILD/OLD

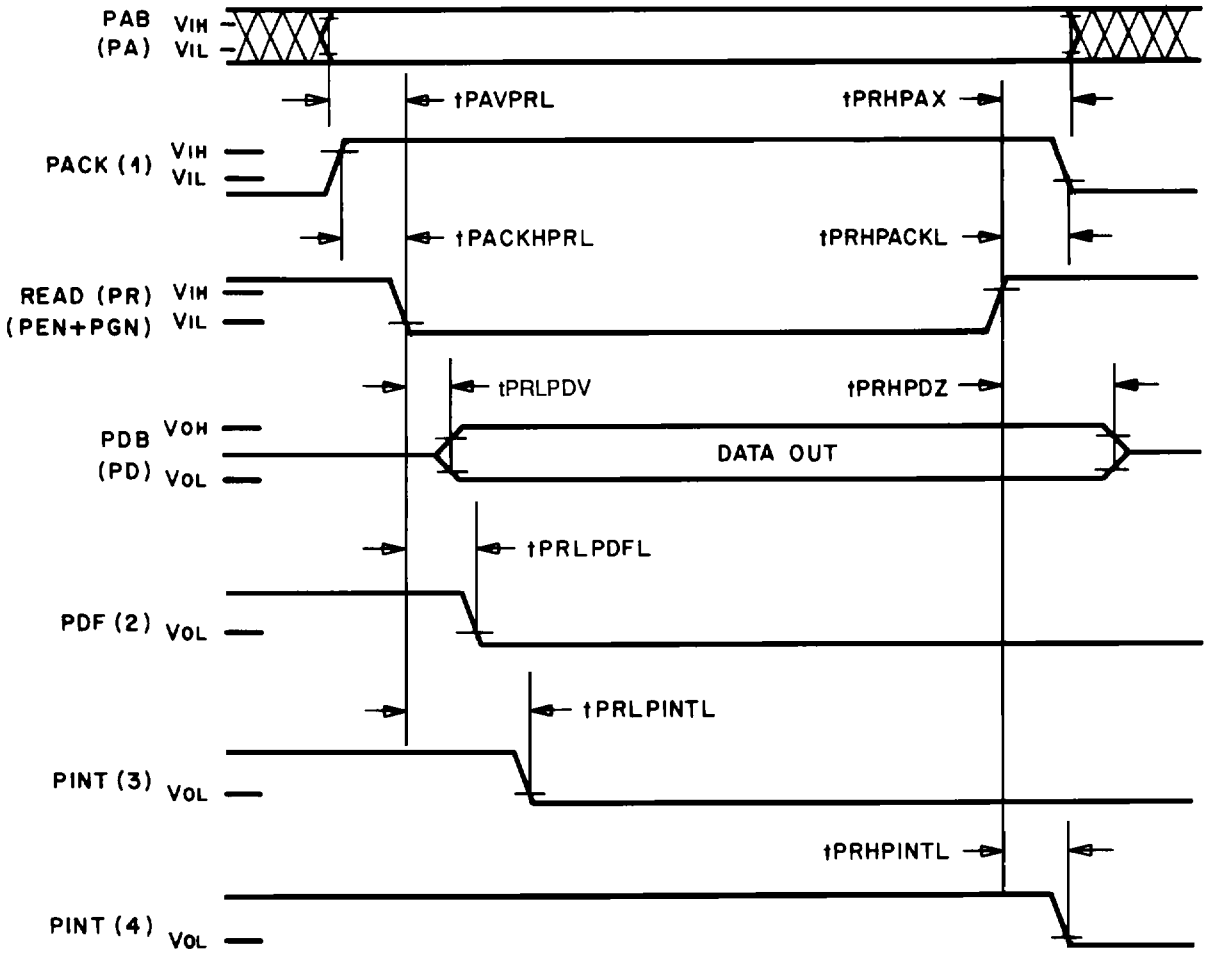


(b) INTERNAL ILD/OLD/SY. EXTERNAL ICK/OCK



(c) INTERNAL ICK/OCK

Figure 17. I/O Clock Generation Timing



Notes:
[1] PACK used only for PIR read. To read other registers, PACK must be 0.
[2] PDF changes only on PAB = 3.
[3] PINT changes for the PIR read (if PINT = 1 is caused by loading of the PIR).
[4] PINT changes for the ESR read (if PINT = 1 is due to unmasked error).

Figure 18. PIO Timing — Read Cycle

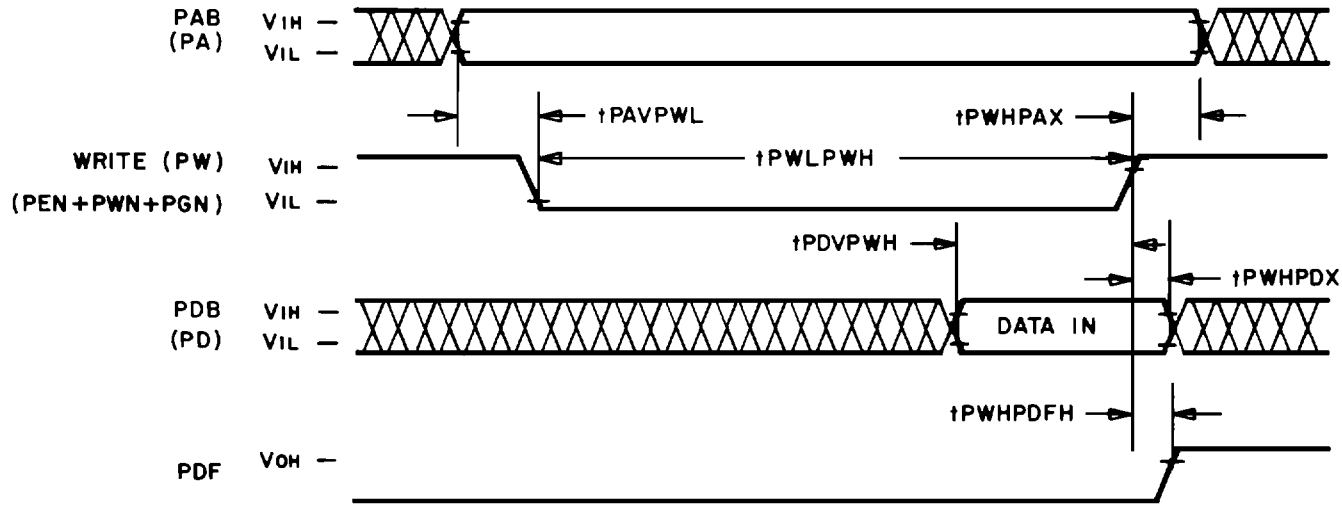


Figure 19. PIO Timing — Write Cycle (PGN High)

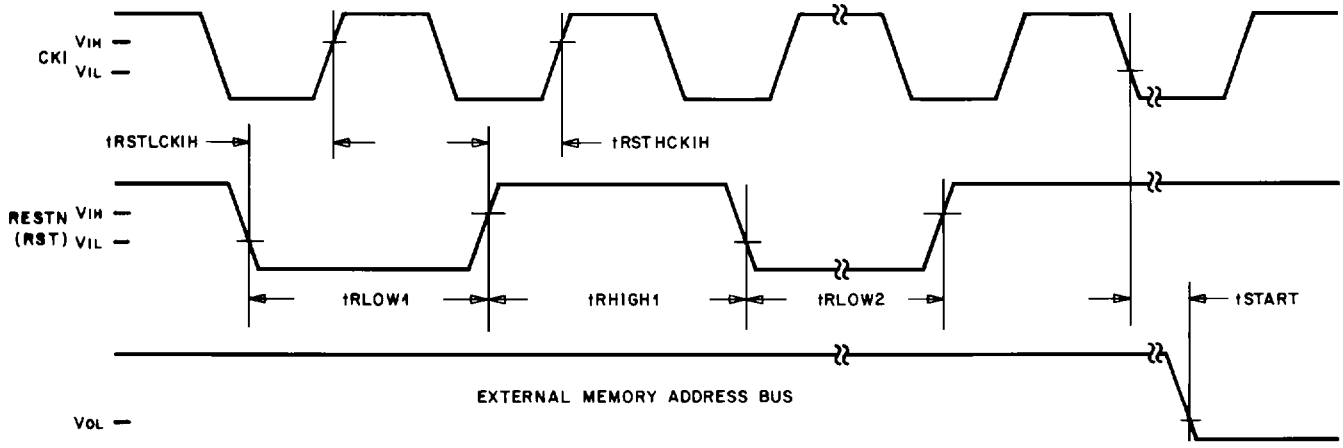


Figure 20. RESTN Initialization Sequence

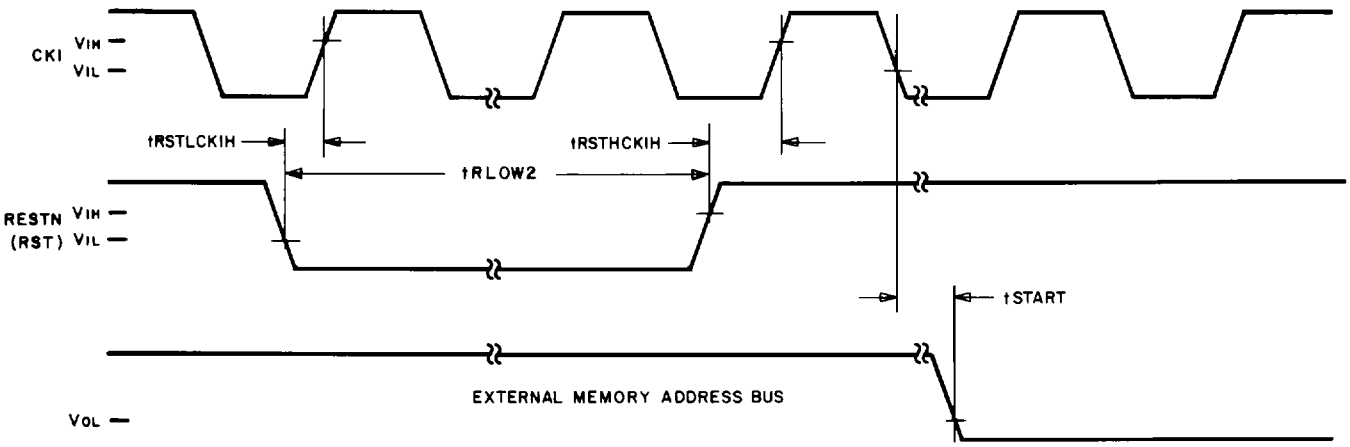
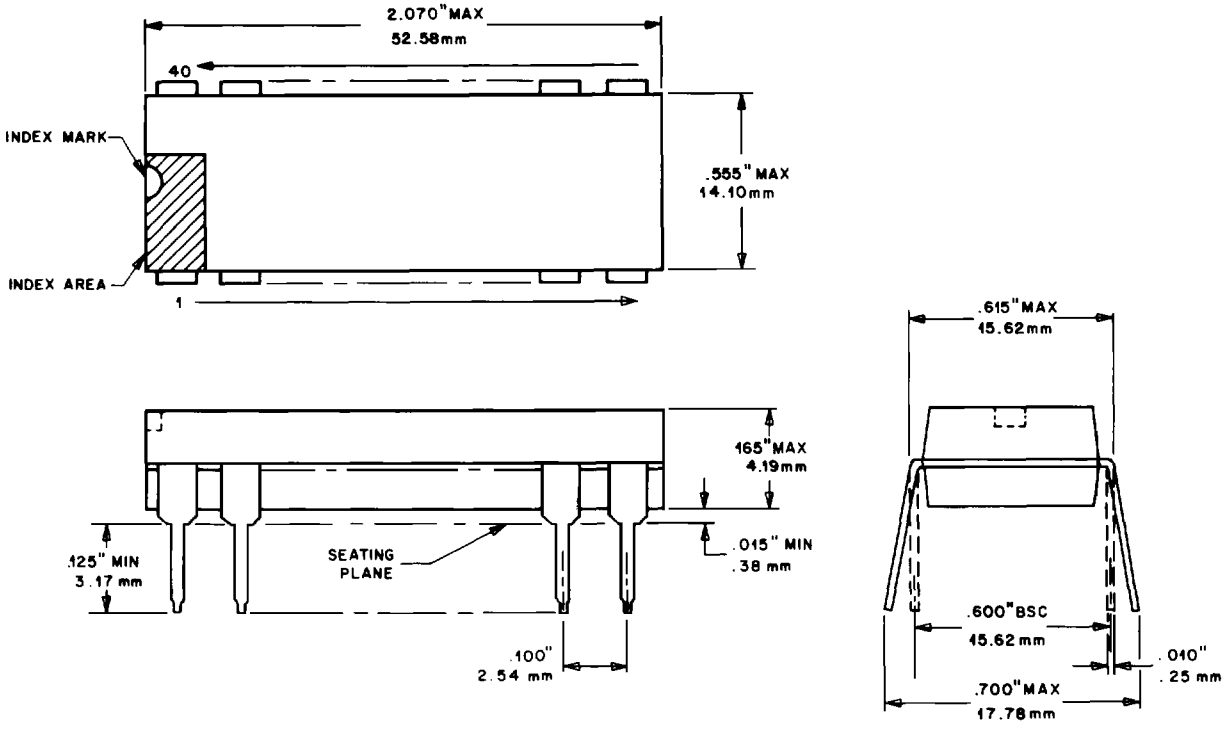


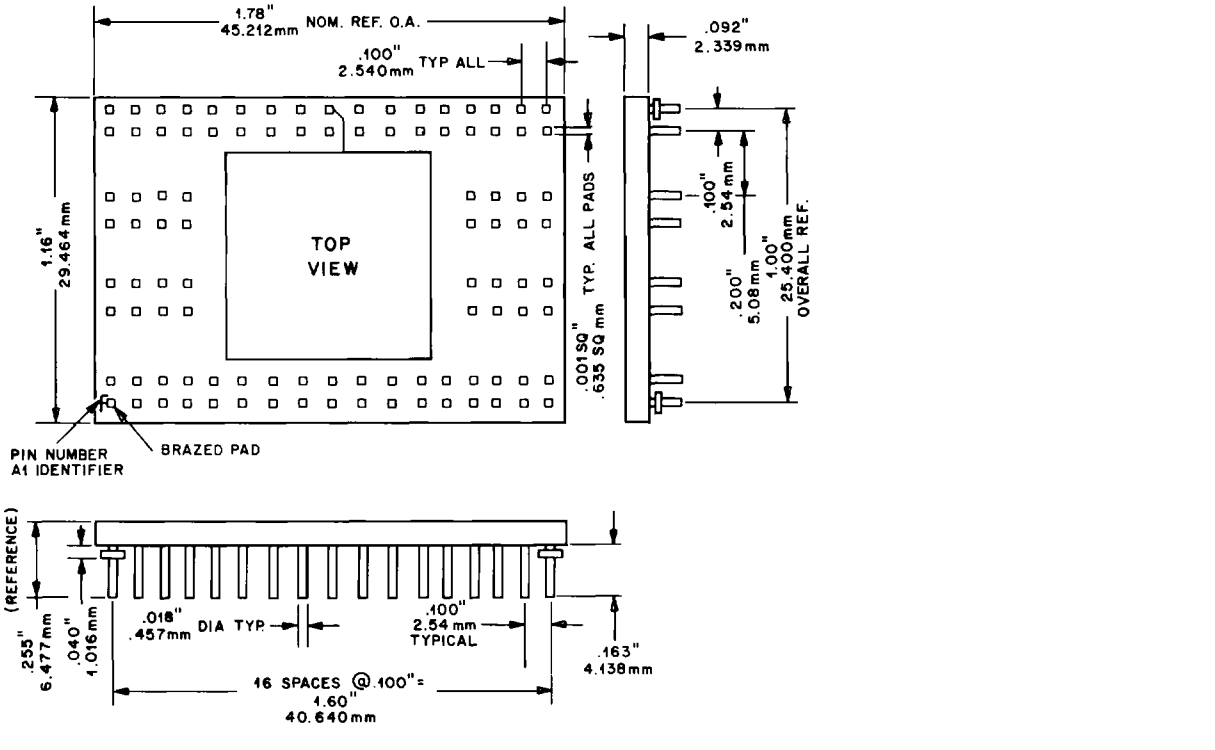
Figure 21. RESTN Halt

Outlines

40-Pin DIP

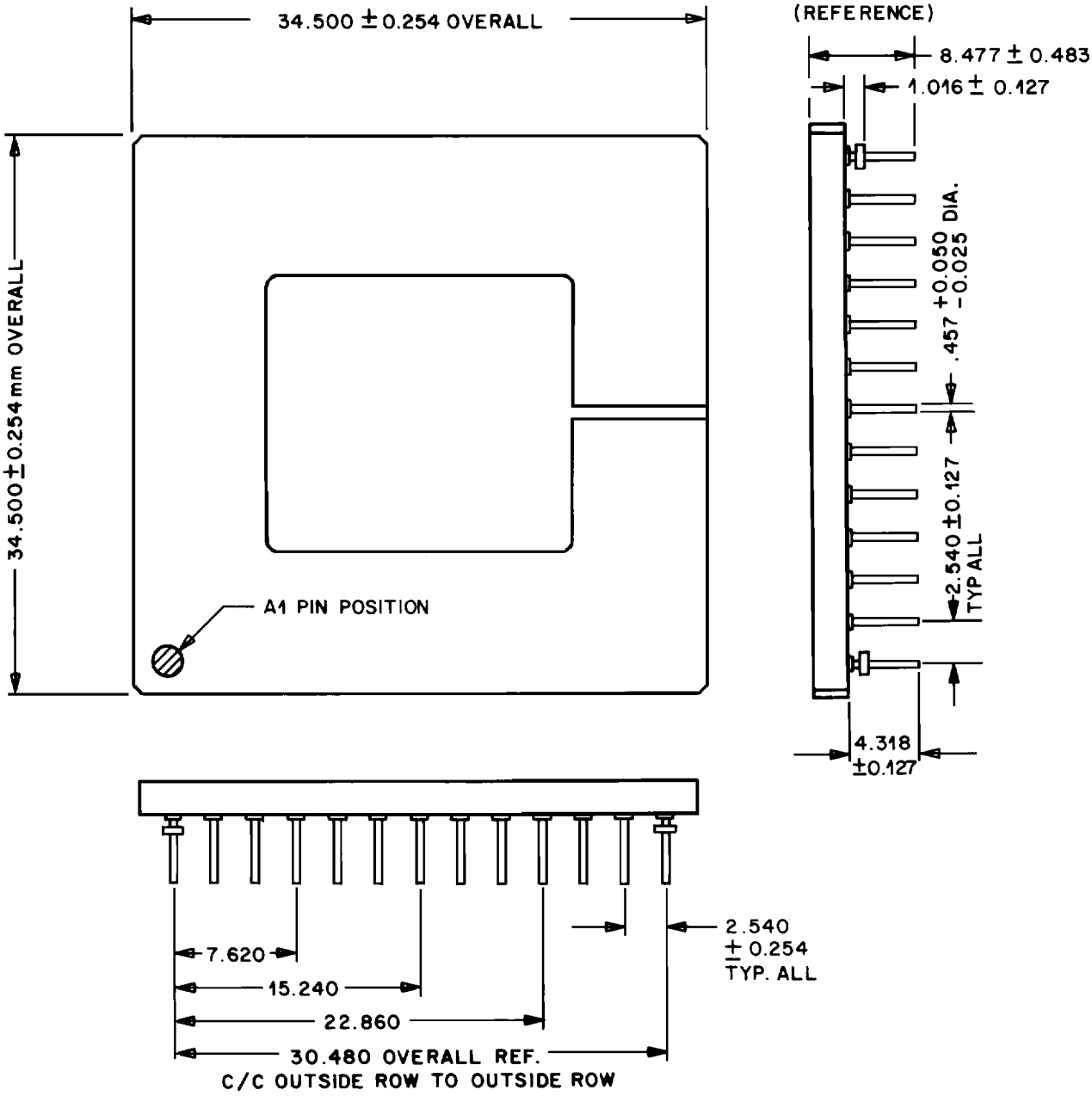


100-Pin PGA Package



13- x 13-Pin Square PGA Package

Dimensions are in millimeters.



Notes

For additional information, contact your AT&T Account Manager, or call:

- AT&T Microelectronics
  Dept. 51AL230230
  555 Union Boulevard
  Allentown, PA 18103
  1-800-372-2447

  In Canada, call:
  1-800-553-2448

- AT&T Microelectronics GmbH
  Freischützstrasse 92
  D-8000 Munich 81
  West Germany
  Tel. 0 89/95 97 0
  Telex 5 216 884

- AT&T Microelectronics Pte. Ltd.
  745 Lorong 5 Toa Payoh
  Singapore 1231
  Tel. 259-6622
  Telex RS42898
  FAX 259-2244

- AT&T Japan
  7F, Fukoku Seimei Bldg.,
  2-2-2, Uchisaiwai-cho,
  Chiyoda-ku, Tokyo 100 Japan
  Tel. (03) 502-3055
  Telex J32562 ATTIJ
  FAX (03) 593-3307

March 1988

DS88-64DMOS